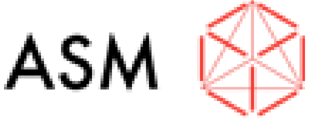
FOW/PLP Consortium

Kick-off meeting



Fan-Out Wafer/Panel-Level Packaging (FOW/PLP) Consortium

(9:30 – 16:30, September 8, 2016)

Unimicron (欣興電子)
No. 290, Chung-Lun Village, Hsinfeng, Hsinchu
(新竹縣新豐鄉中崙村290號)

AGENDA

9:30 – 9:35 Welcome (TJ Tseng, Chairman, Unimicron)
9:35 – 9:40 Welcome (Nelson Fan, Vice President, ASM-HK)
9:40 – 9:50 Self-introduction (all participants)
9:50 – 10:45 Objectives, scope, key tasks, approach, deliverables, IP issues, communication methods, membership fee (all participants)
10:45 – 11:00 Tea break (all participants)
11:00 – 12:30 Key capability of each participant company (≤15 minutes for each company)
12:30 – 1:30 Lunch (all participants)
1:30 – 3:00 Test vehicles (all participants)
3:00 – 3:10 Tea break (all participants)
3:10 – 3:50 Test vehicles and company task assignments (all participants)
3:50 – 4:30 Plant tour (all participants)
4:30 - So long (all participants)

FOW/PLP Consortium

Chip-First (die-up and die-down) Fan-Out Wafer/Panel-Level Packaging (FOW/PLP)

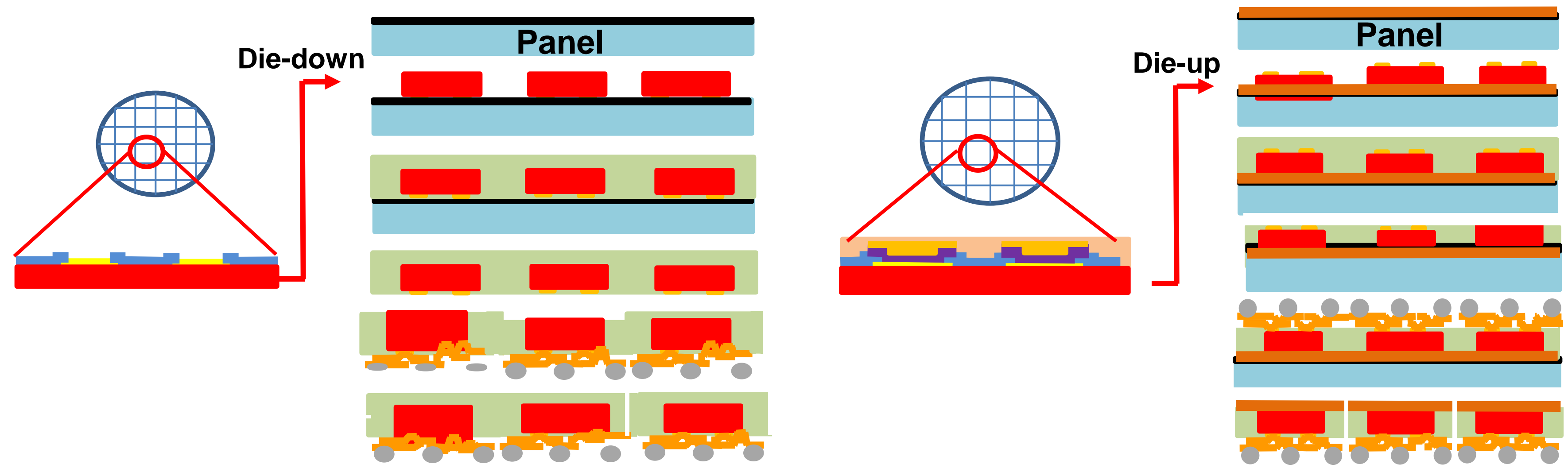
ASM

FOW/PLP Consortium Project

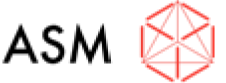
Title: Chip-First (die-up and die-down) FOW/PLP

Duration: 24 months

Fee: US$50,000*



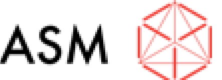
*Please see The Rights and Fee of FOPLP Consortium Members.



PURPOSES

The objective of the consortium is to develop low-cost and high-throughput manufacturable processes for FOW/PLP with emphasis on:

(a) WLSiP (wafer-level System-in-Package) and PLSiP (panel-level System-in-Package)
(b) P&P (pick & place) technology
(c) Low-warpage molding
(d) RDLs (redistribution-layers) technology
(e) Line width and spacing



Fan-Out Wafer/Panel-Level Packaging (FOW/PLP)

EMC

CHIP1

CHIP2

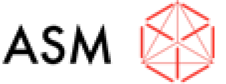
Pad

RDLs

Pad

Solder ball

Printed Circuit Board (PCB)



SCOPES

Panel Sizes:

- ❑ 340mmx340mm (area: 1.6 times of 12”wafer)
- ❑ 457mmx610mm (area: 3.8 times of 12”wafer)

Wafer Size:

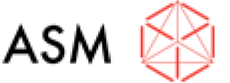
- ❑ 300mm

Line width/Spacing ≥10μm:

- ❑ Formation is chip-first with die-down
- ❑ P&P use high-precision and SMT equipment
- ❑ RDLs use PCB + LDI (laser direct imaging) technology
- ❑ RDLs use polymer +ECD

Line width/Spacing <10μm:

- ❑ Formation is chip-first with die-up
- ❑ P&P use high-precision equipment
- ❑ RDLs use polymer + ECD



Key Tasks

➢ Design of Test Vehicles

- ❑ Electrical design & characterization of FOW/PLP
- ❑ Structural design and optimization of FOW/PLP
- ❑ Thermal design and optimization of FOW/PLP

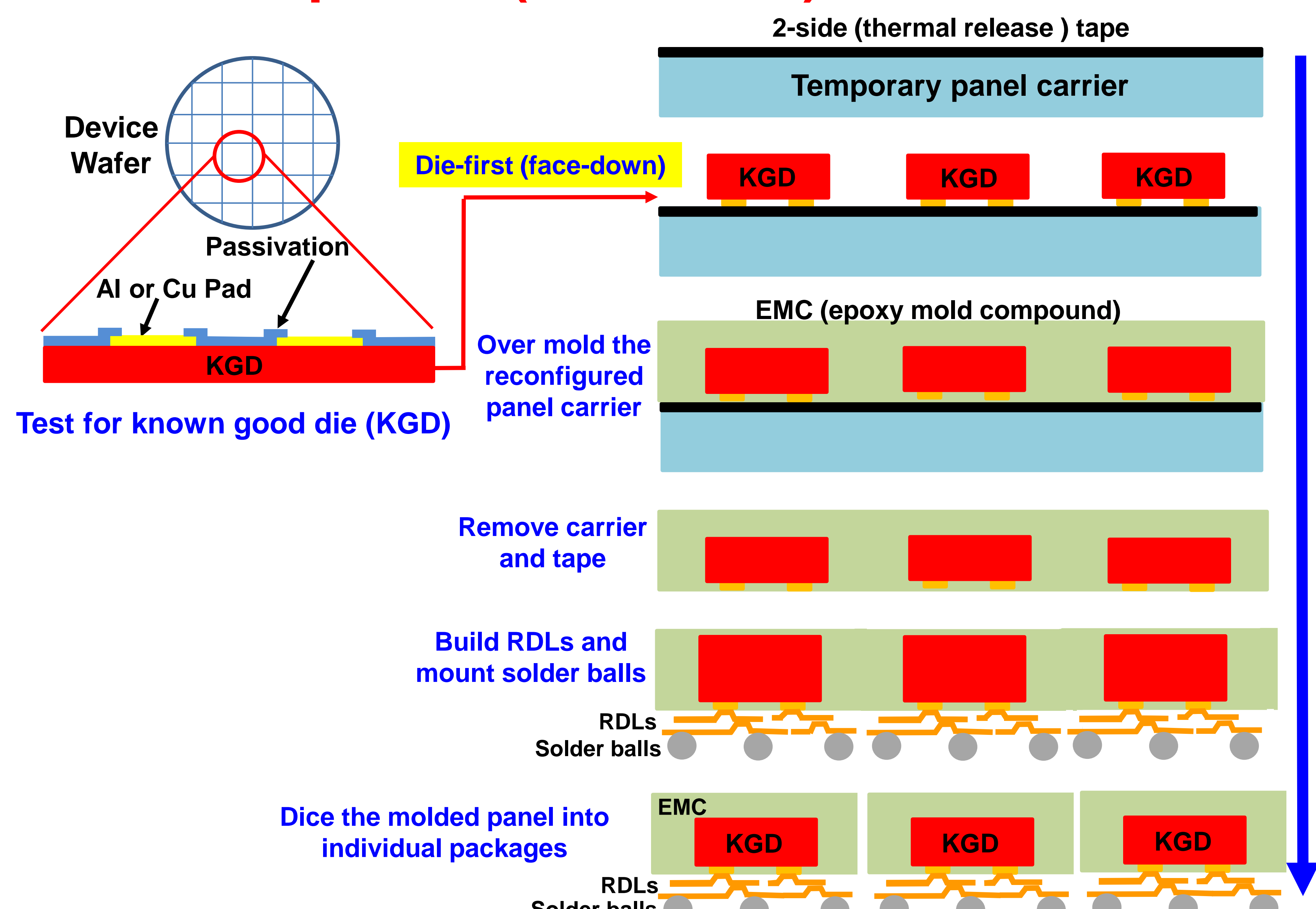
➢ FOPLP Technology

- ❑ P&P process development
- ❑ Compression molding process development
- ❑ Redistribution layer (RDL) process development
- ❑ Solder ball mounting
- ❑ Material selections
- ❑ Warpage Control

➢ Assembly and Reliability

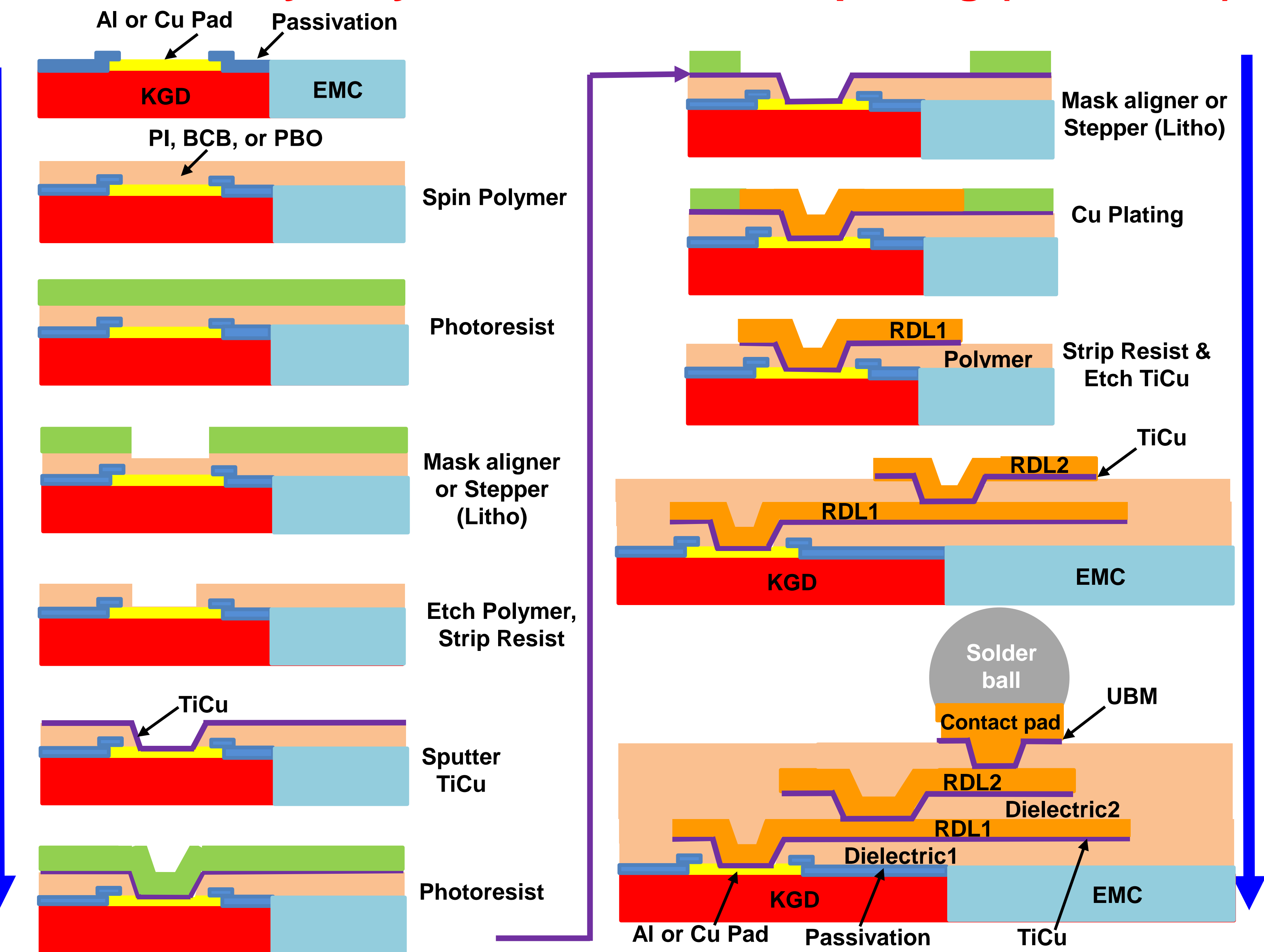
- ❑ PCB Assembly processes development
- ❑ Testing Characterizations
- ❑ Reliability assessment and failure analysis

Chip-First (Die-Down) FOW/PLP

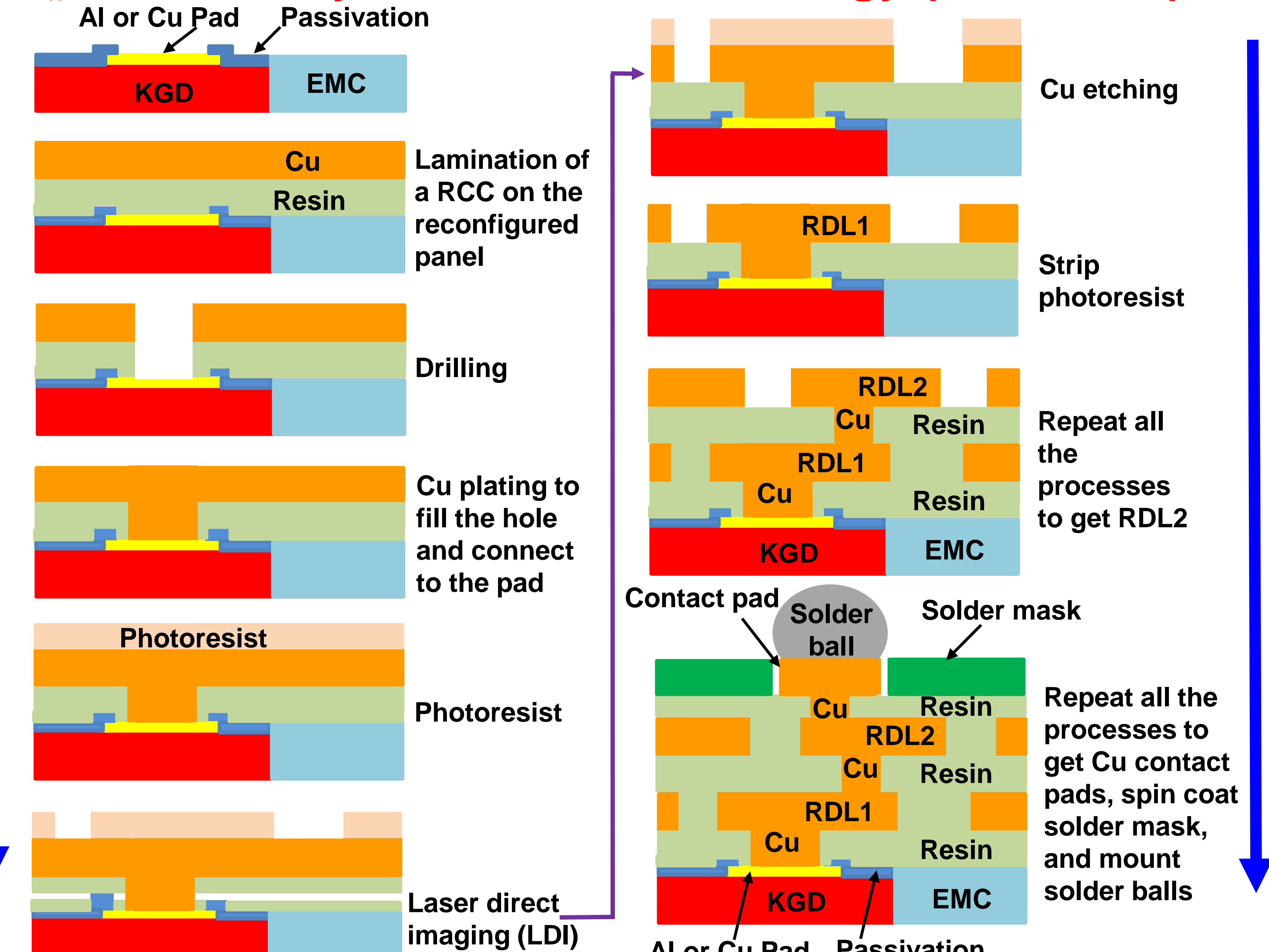


ASM

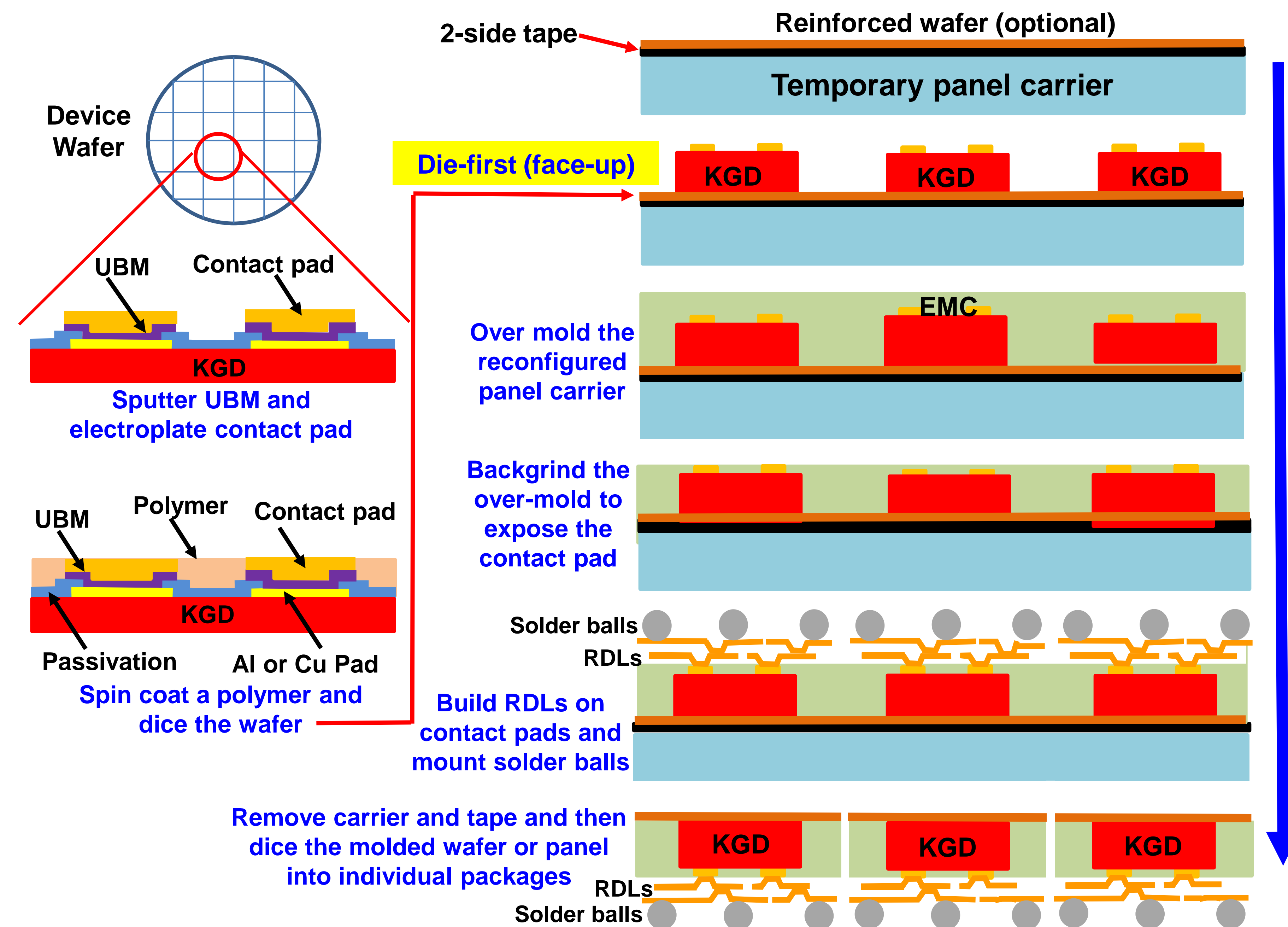
RDLs by Polymer and Cu Electroplating (Die-Down)



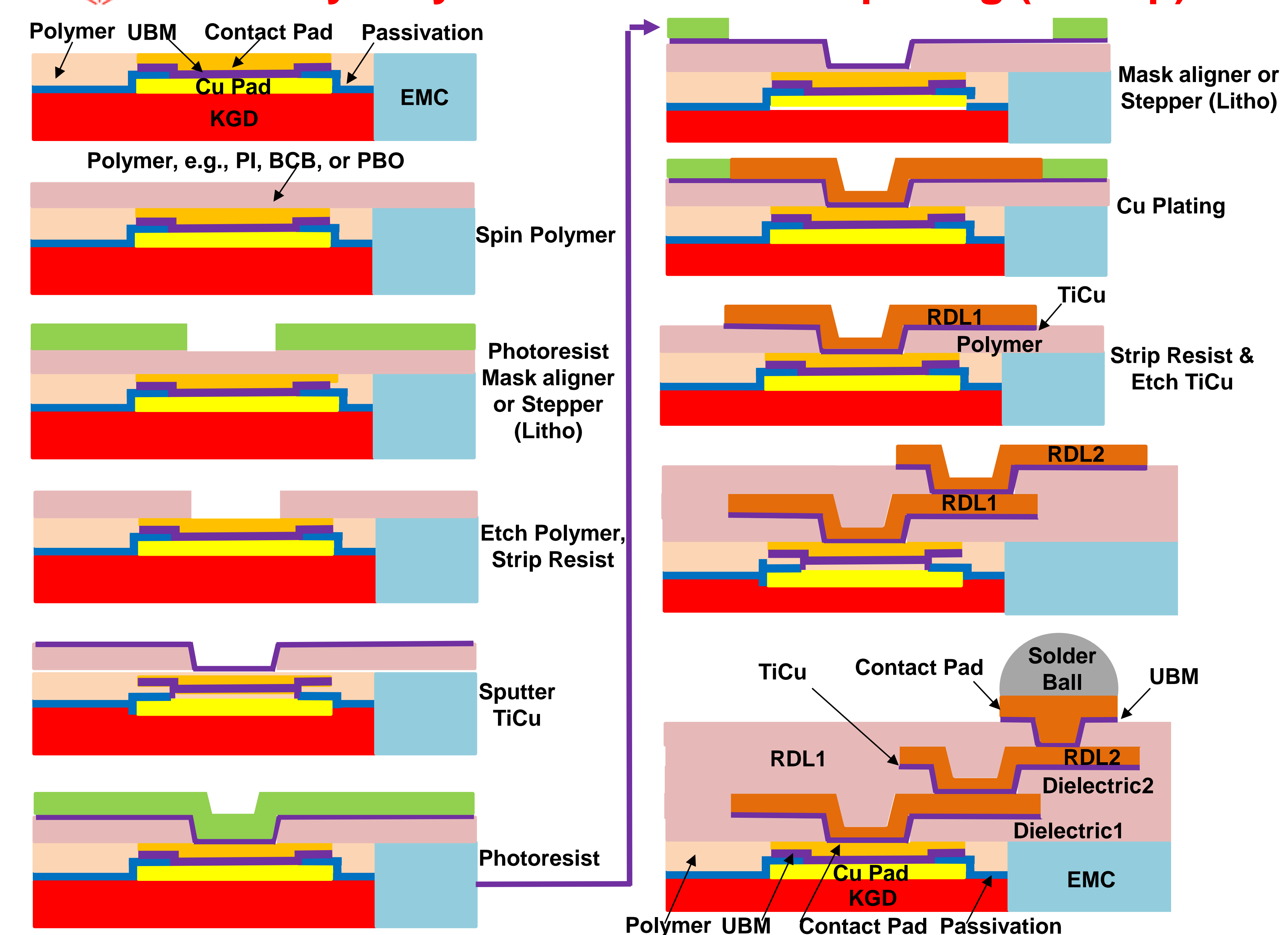
RDLs by PCB + LDI Technology (Die-Down)



Chip-First (Die-Up) FOW/PLP



RDLs by Polymer and Cu Electroplating (Die-Up)



APPROACH

Members input → **Finalize FOW/PLP project scope and test vehicle specification**

↓

Electrical/Thermal design

↓

- **P&P development**
- **Molding process development**
- **RDL process development**

↓

Test vehicle fabrication

- → **Electrical characterization** (feeds back to Electrical/Thermal design)
- → **Quick reliability assessment** (feeds back to Electrical/Thermal design)

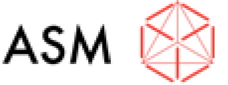
↓

Design/process/assembly Improvement

↓

Final test vehicle fabrication and assembly

- → **Final electrical/ Thermal characterization**
- → **Final reliability test and failure analysis**

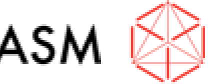


DELIVERABLES

- Design guidelines of using FOW/PLP.
- Materials guidelines of using FOW/PLP.
- Process guidelines (such as P&P, molding, RDLs, ball mounting, dicing, and PCB assembly) of using FOW/PLP.
- Electrical modeling results and characterization data for FOW/PLP.
- Mechanical & thermal modeling results and optimization for FOW/PLP.
- Reliability data and failure analysis report of FOW/PLP.
- Cost models for FOW/PLP.
- The limitations of FOW/PLP.

IP Issues

- In order to use a prior-art IP (intellectual property), it has to be voted on by a simple majority by the members of this consortium prior to its use.
- The title, and interest to any IP developed during the course of this project development shall be owned and the cost of all IPs will be shared by the members of this consortium who have contributed to the development of the IP.
- Notwithstanding the foregoing, all the members of this consortium (including those who have not contributed to the development of the IP during the course of this project development) shall have the right to use the IP developed during the course of this project development in their normal course of business without the need to pay any royalty fee for their usage thereof.



Introduction to
ASM FOW/PLP Membership

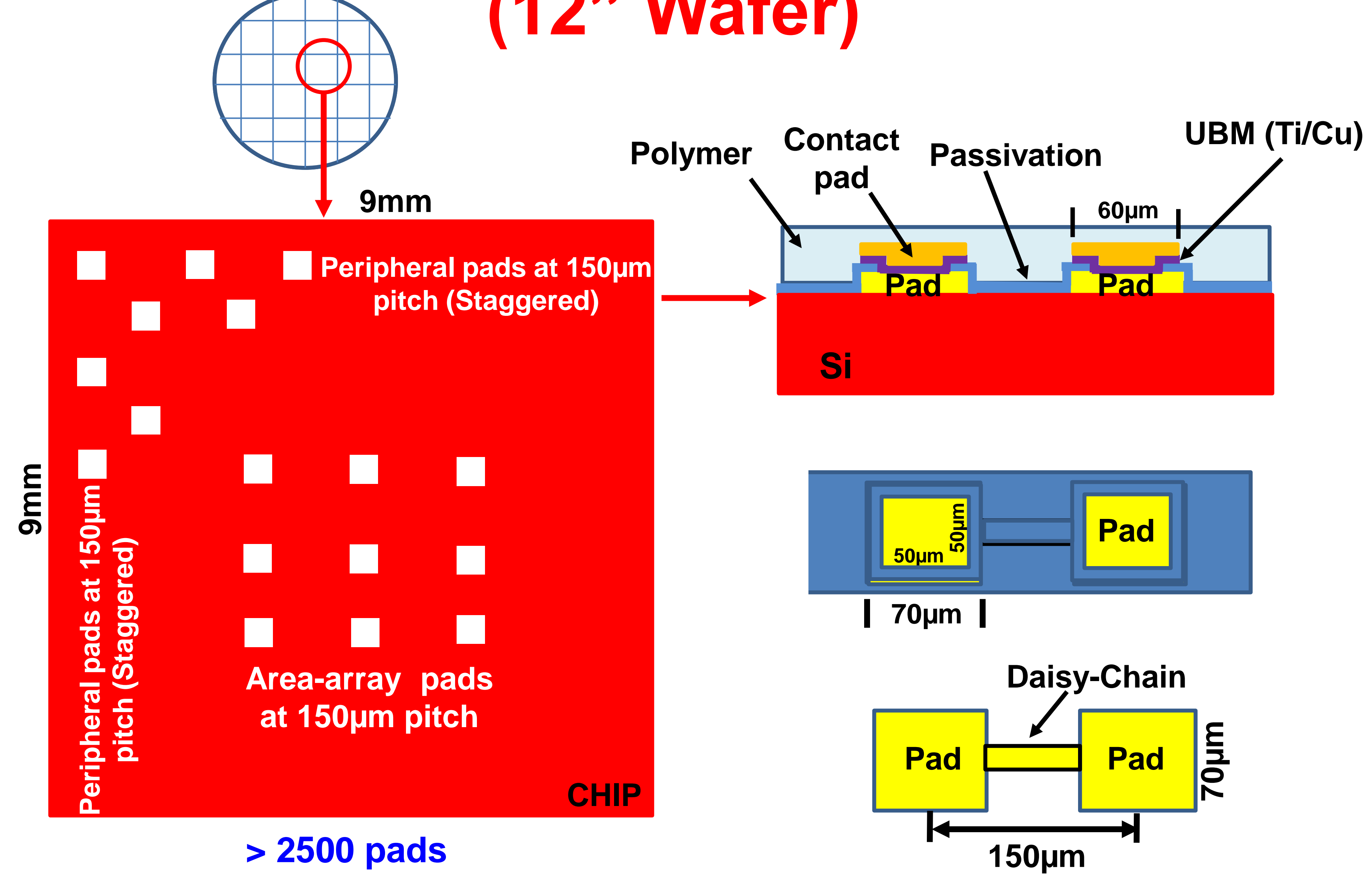
The Rights and Fee of FOW/PLP Consortium Members

1. The FOW/PLP consortium members shall
   - A. have a right to participate any portion of the project.
   - B. have a right to vote on the project expenses, which come from the member fee.
   - C. have a right to jointly work out a future development roadmap for FOW/PLP project and timeframe.
   - D. have a right to attend regular 3-month meeting/discussions of FOW/PLP project.
   - E. have a right to obtain regular FOW/PLP project meetings, minutes, and joint development status report on a monthly basis.
2. Member fee is US$50,000, which covers project materials (e.g., Si-wafer. UBM, and raw materials) and sub-contract (e.g., reliability tests) cost.

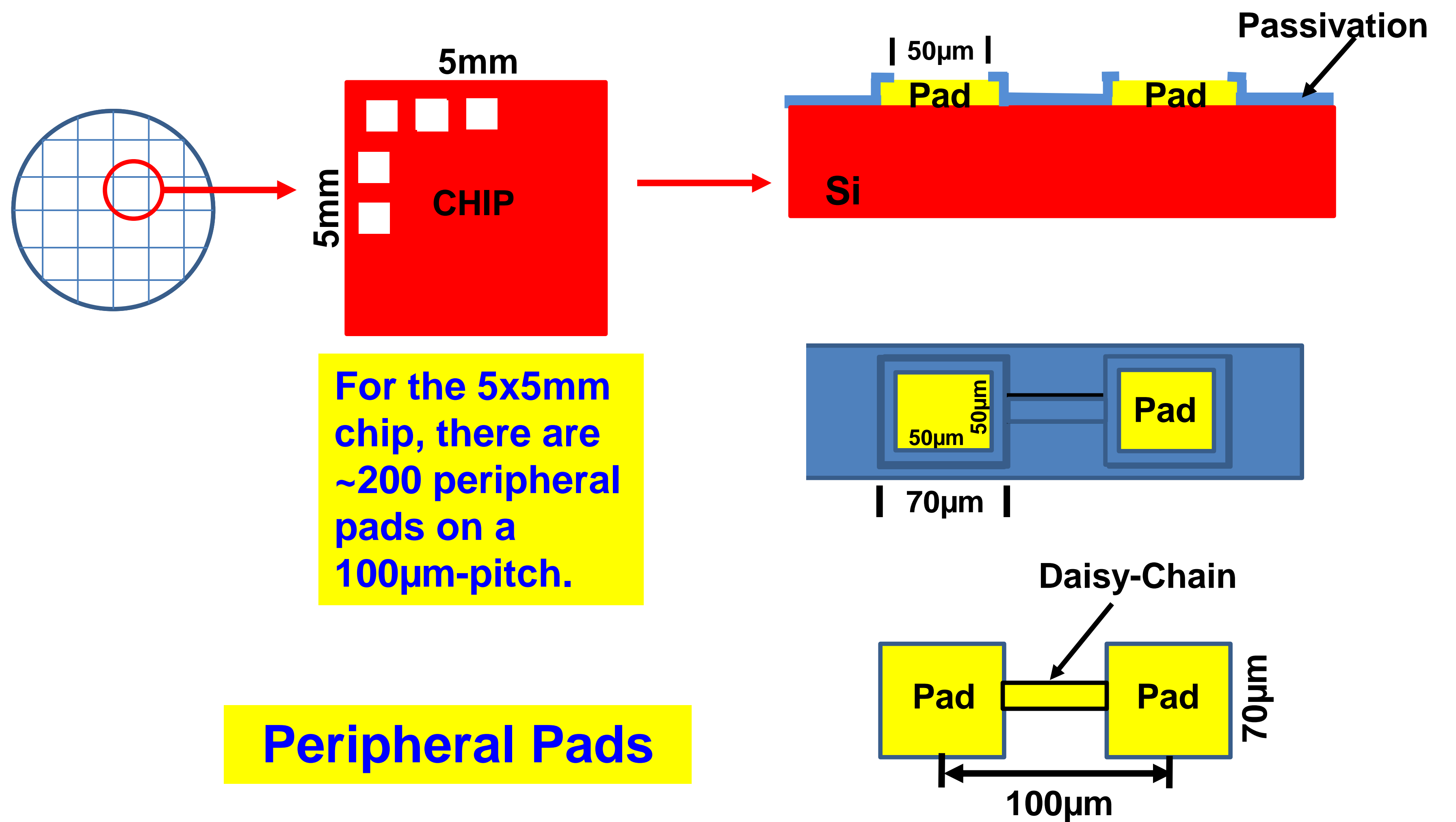
FOW/PLP Consortium

Test Vehicles

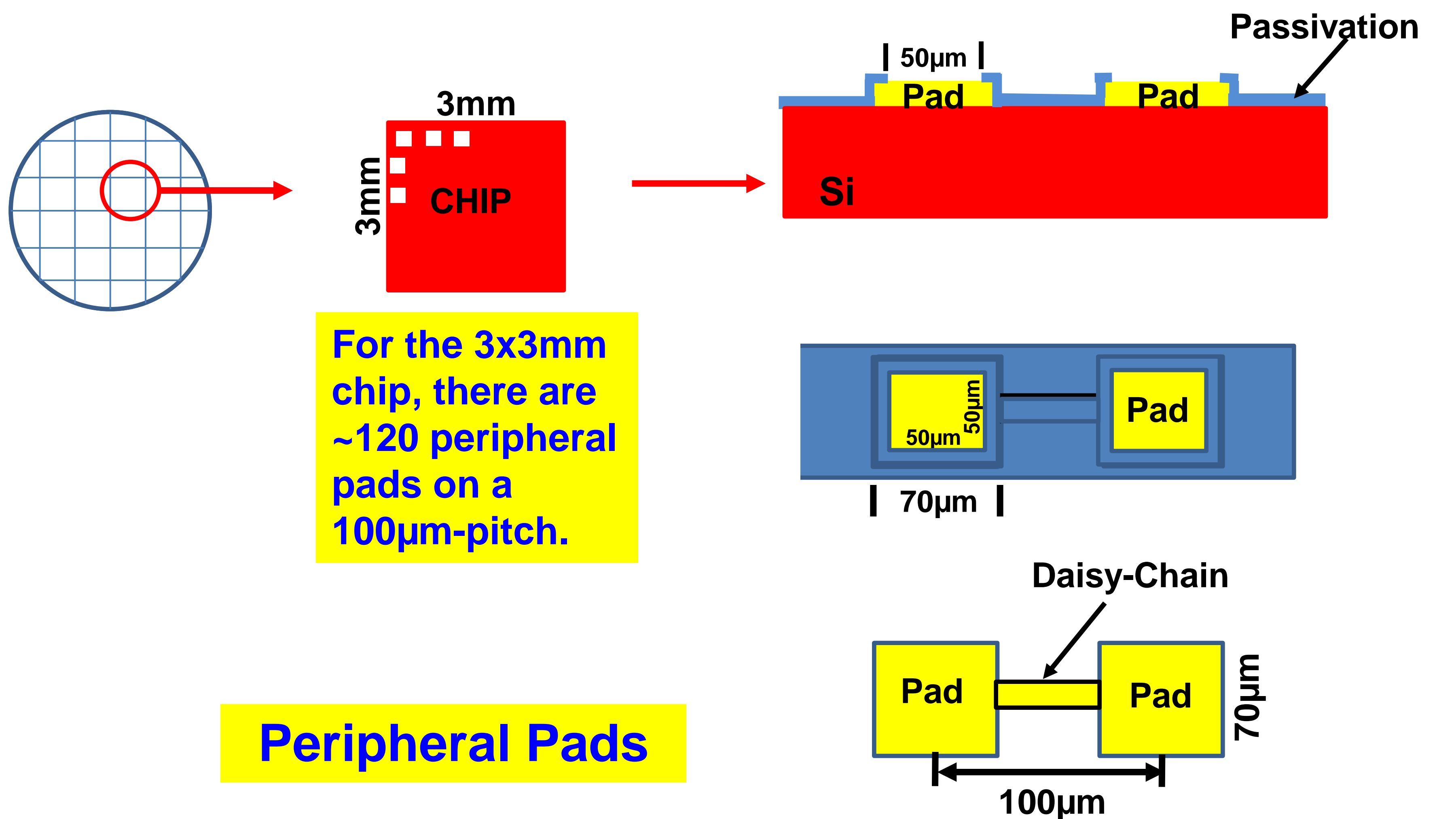
Chip Size (9mm x 9mm) for Test Vehicles (12" Wafer)



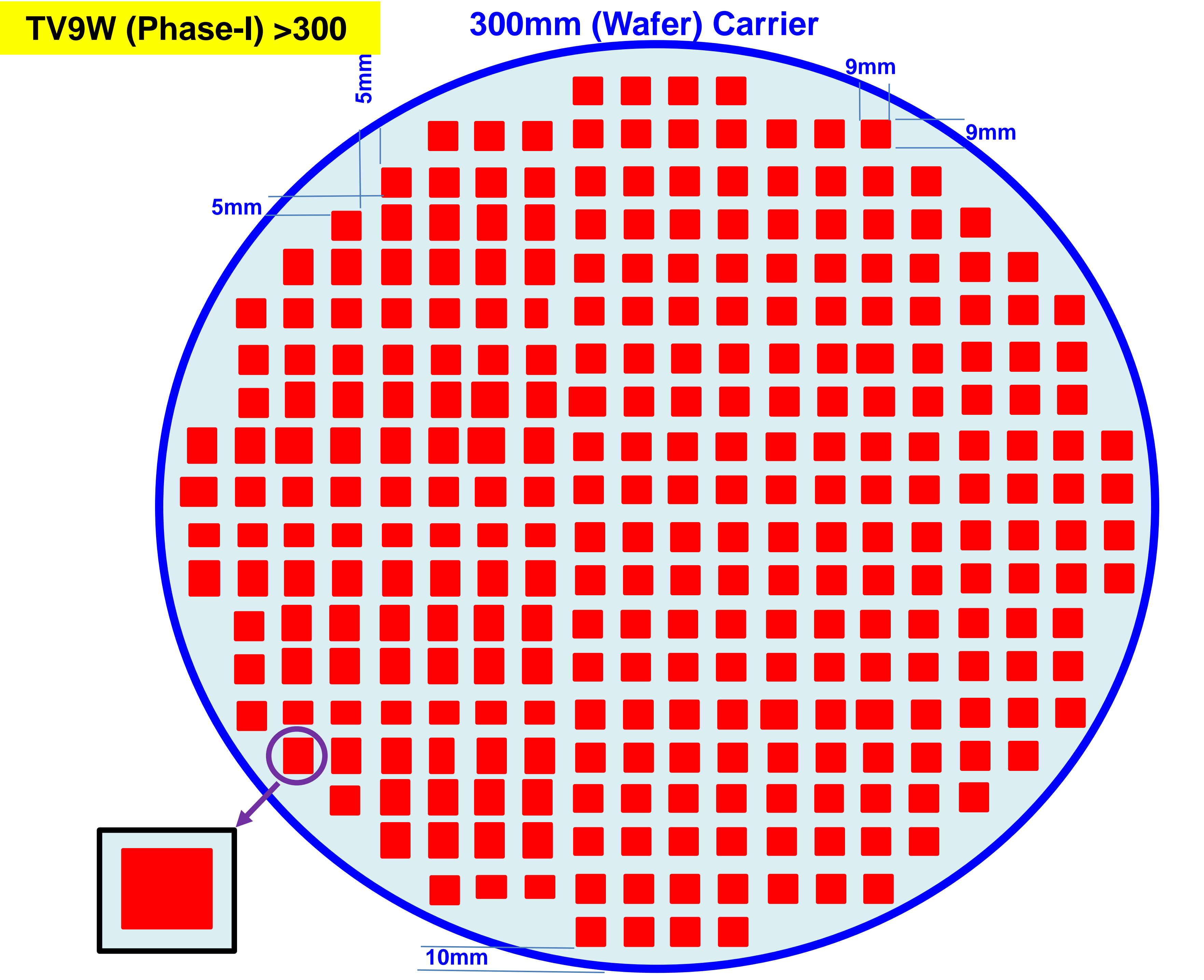
Chip Size (5mm x 5mm) for Test Vehicles (12" Wafer)



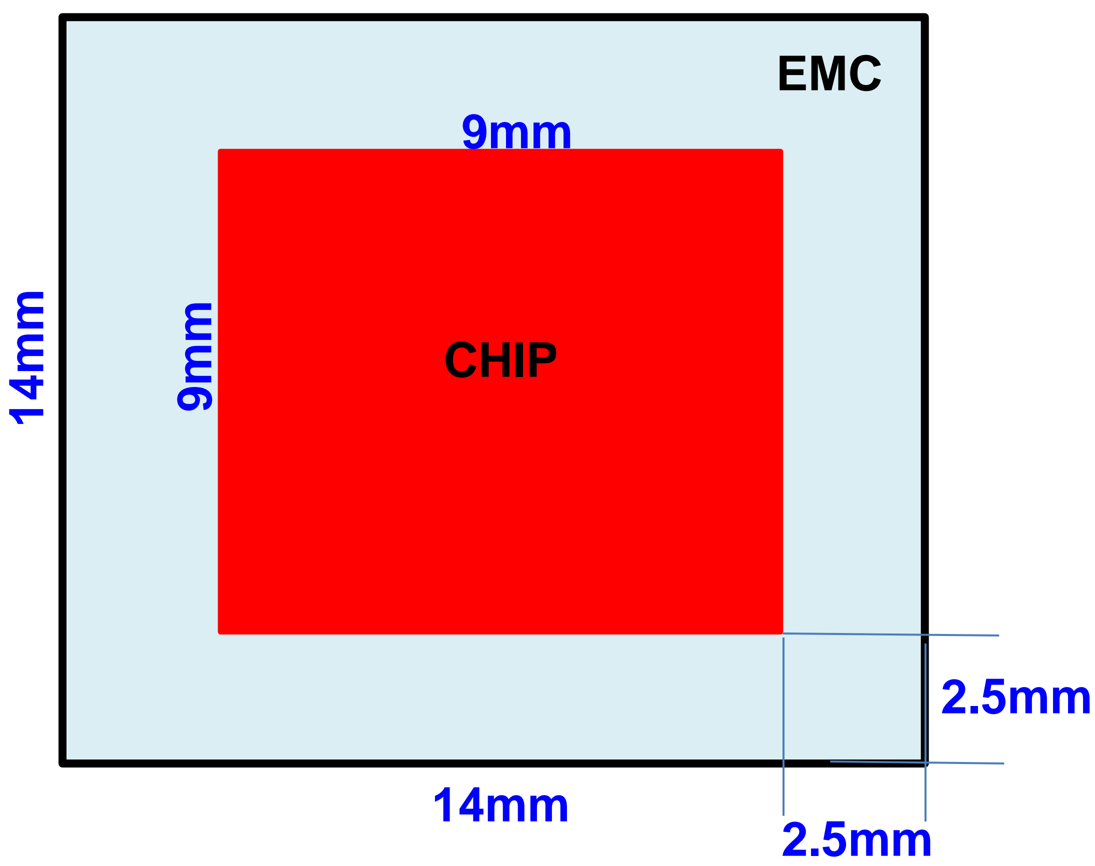
Chip Size (3mm x 3mm) for Test Vehicles (12” Wafer)



Phase - I

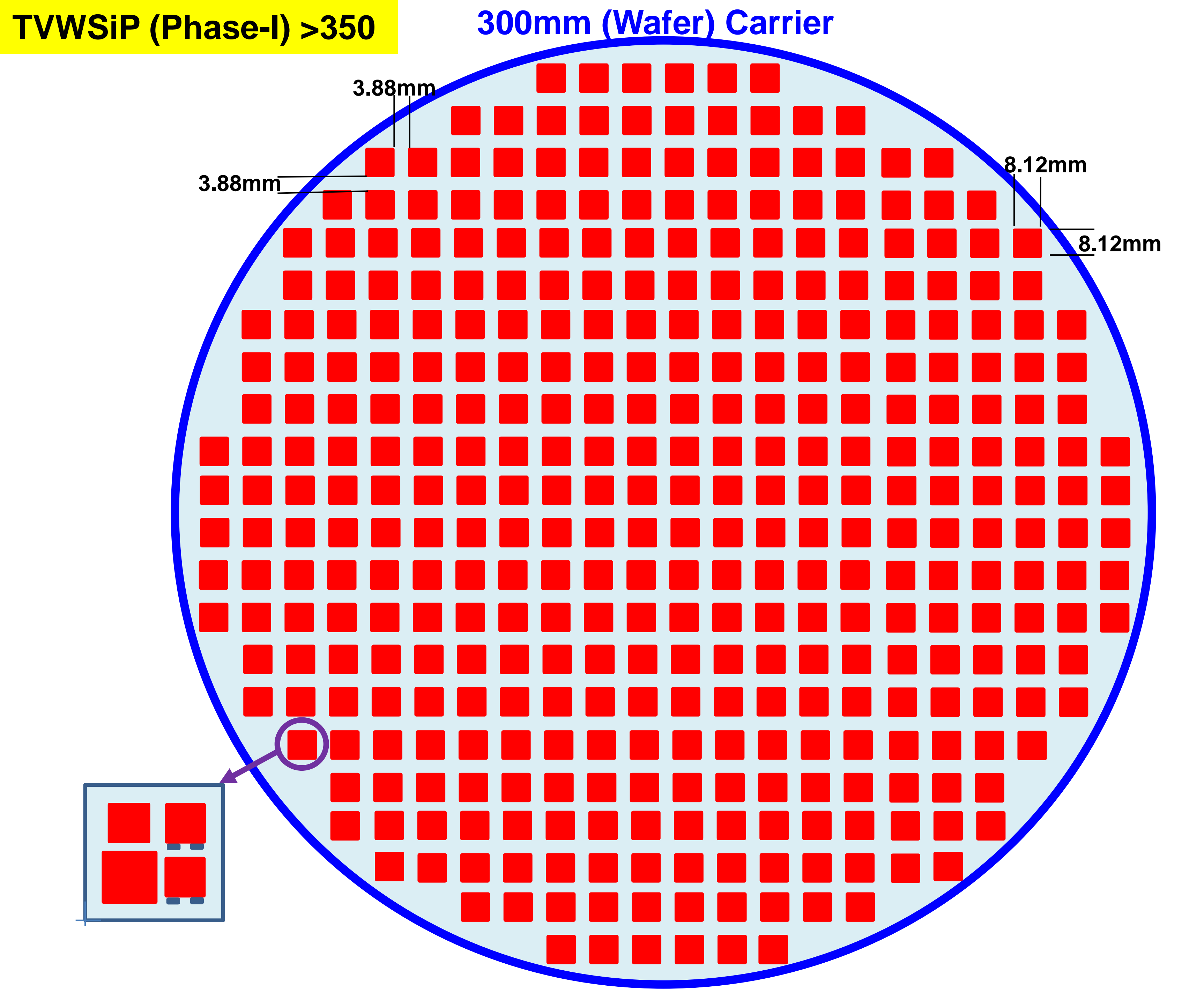

TV9W (Phase-I) >300
300mm (Wafer) Carrier
9mm
9mm
5mm
5mm
10mm

TV9 (Phase-I)



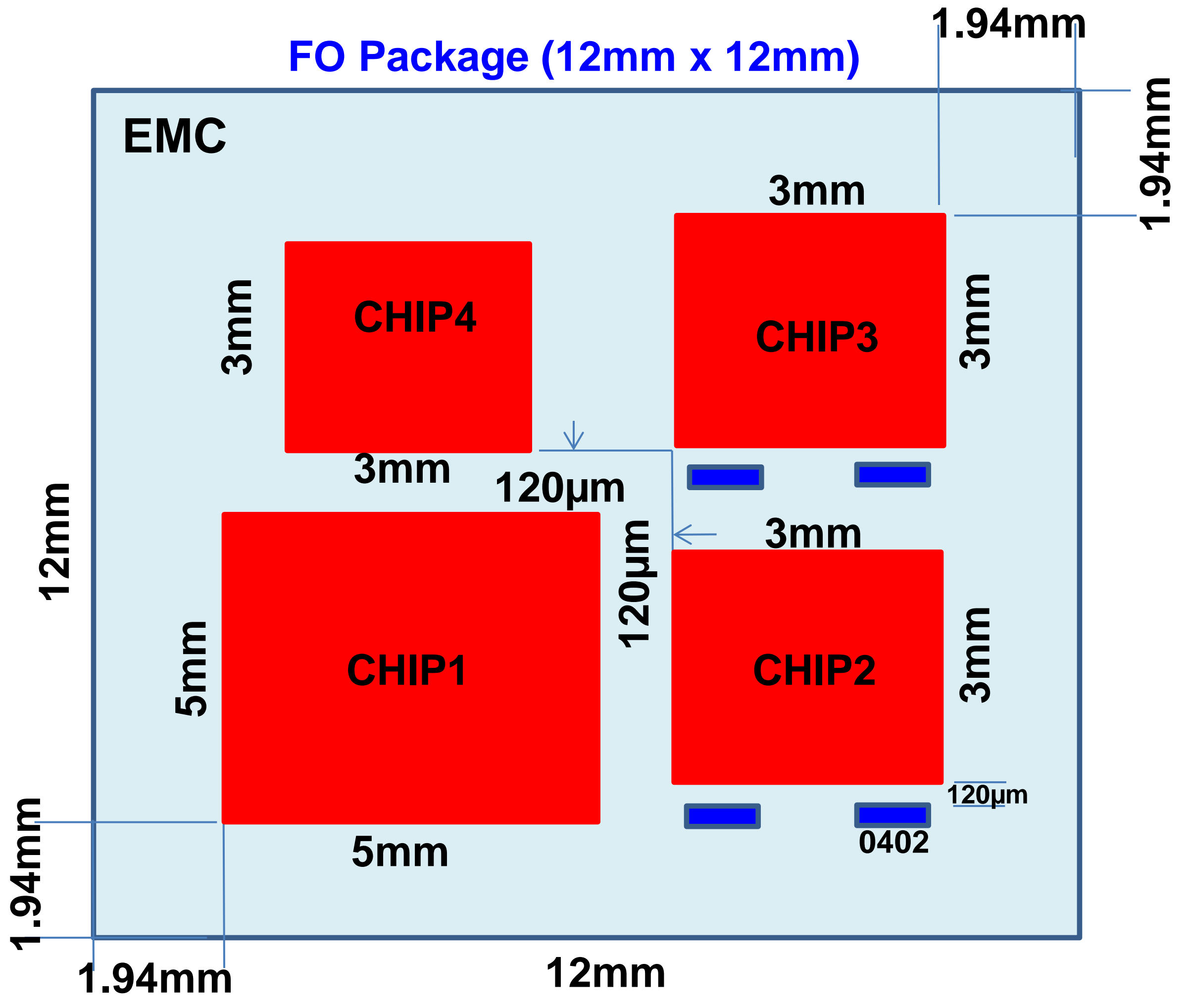
Line width/spacing of:

- 1st RDL are 5/5μm
- 2nd RDL are 10/10μm
- 3rd RDL are 15/15μm



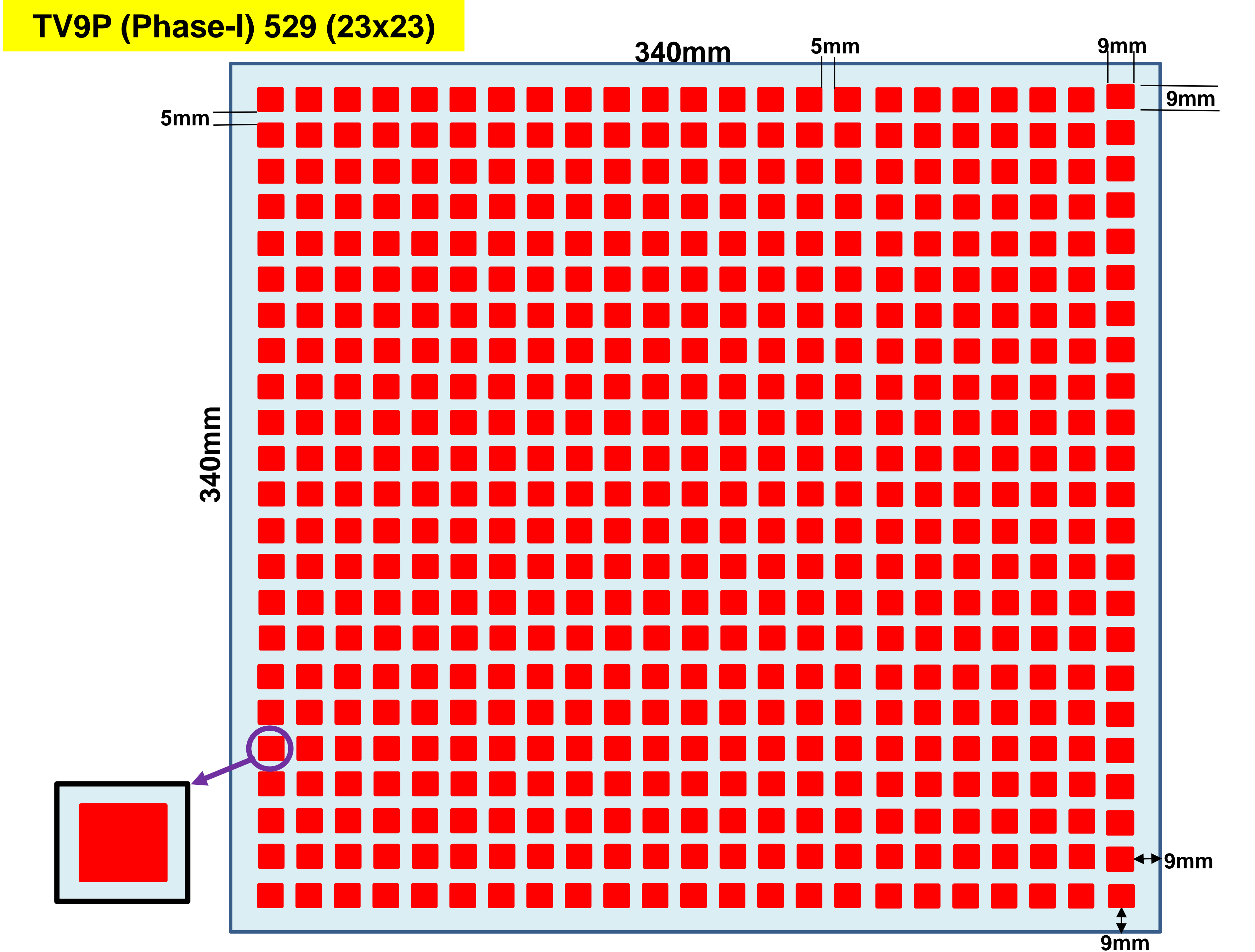
TVWSiP (Phase-I) >350
300mm (Wafer) Carrier
3.88mm
3.88mm
8.12mm
8.12mm

TVSiP (Phase-I)

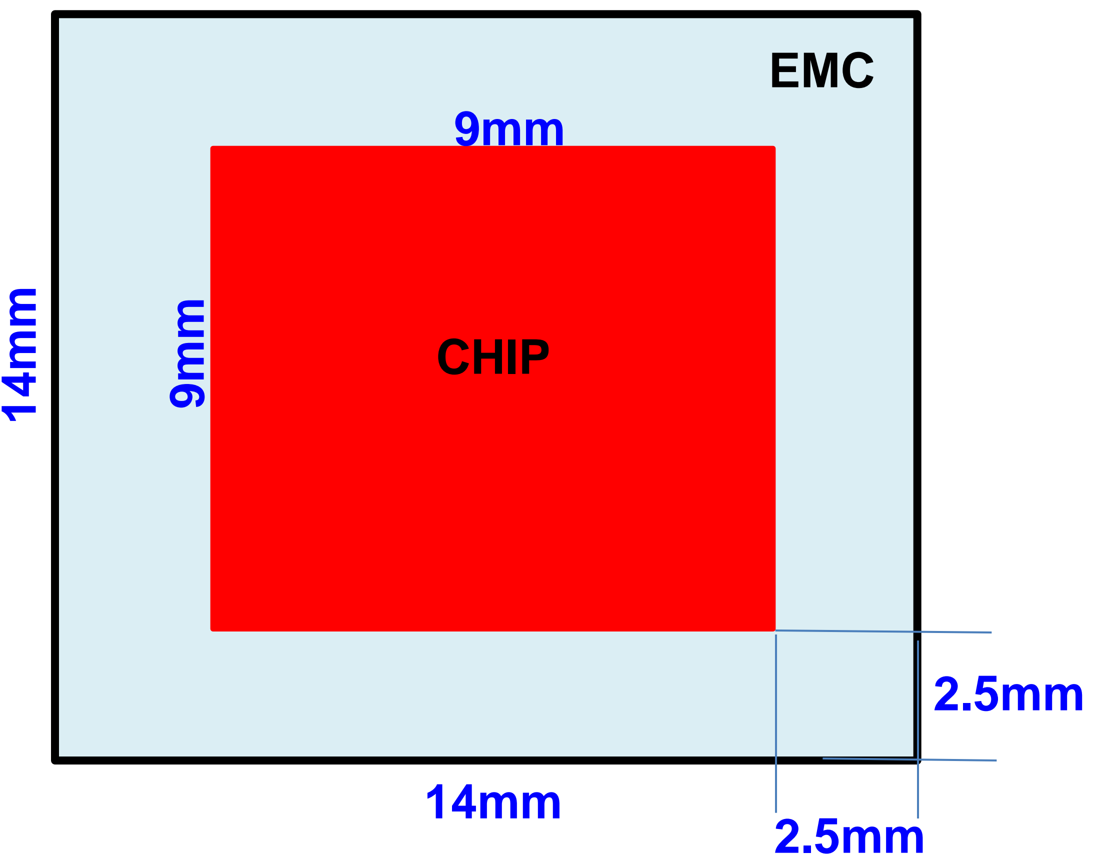


Line width/spacing of:

- 1st RDL are 10/10µm
- 2nd RDL are 15/15µm

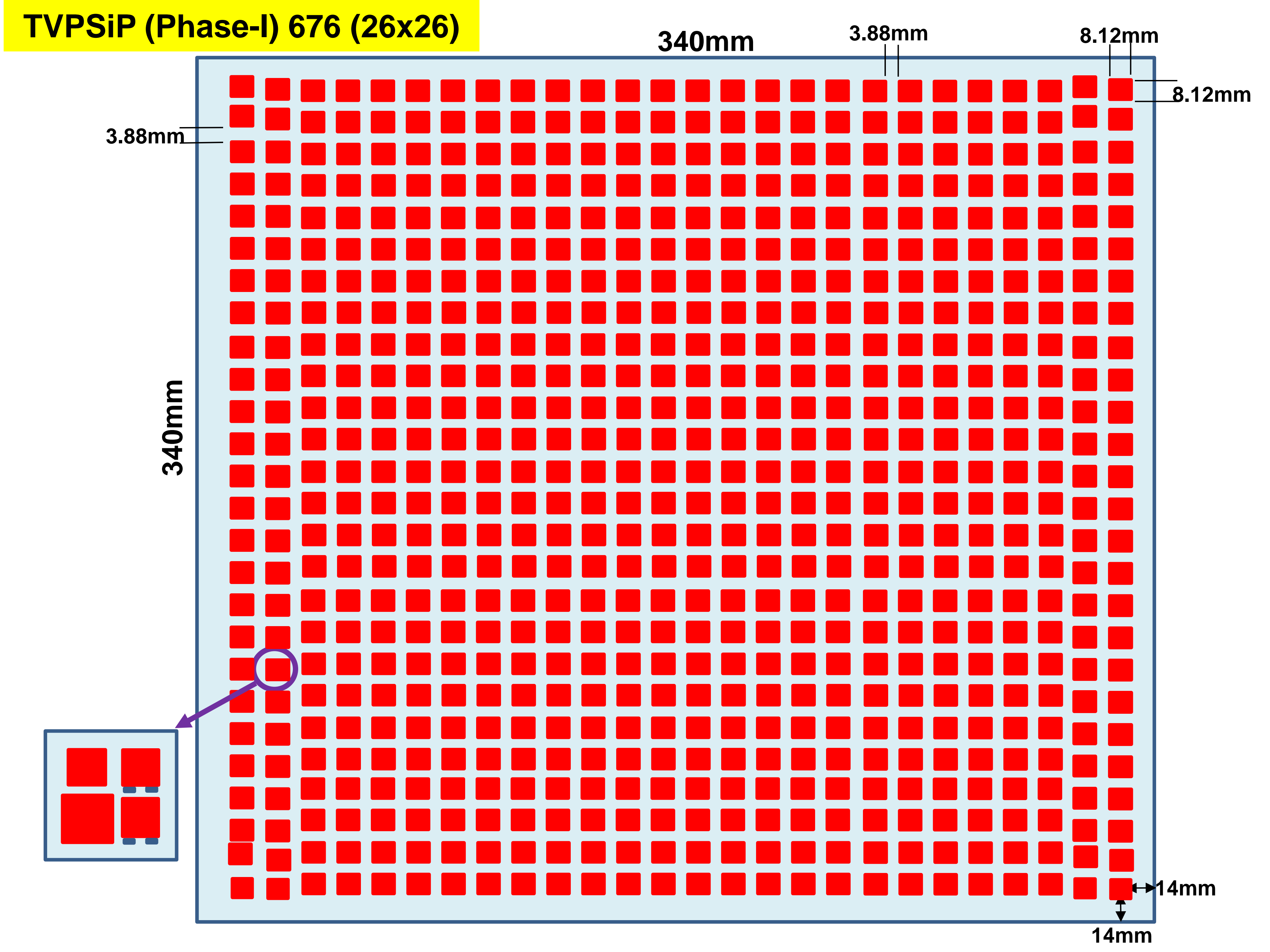

TV9P (Phase-I) 529 (23x23)
340mm
5mm
9mm
9mm
5mm
340mm
9mm
9mm

TV9 (Phase-I)

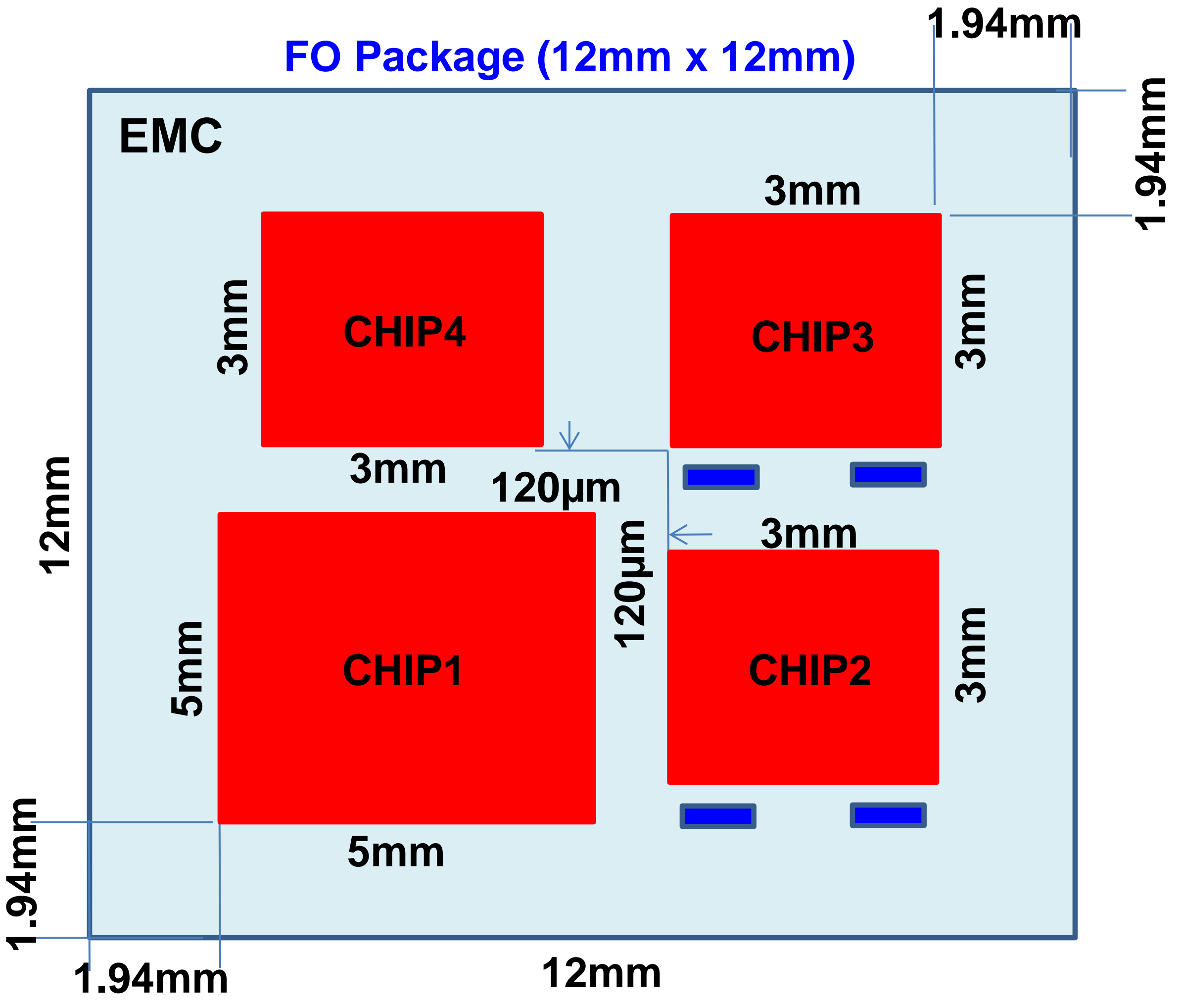


Line width/spacing of:

- 1st RDL are 5/5μm
- 2nd RDL are 10/10μm
- 3rd RDL are 15/15μm


TVPSiP (Phase-I) 676 (26x26)
340mm
3.88mm
8.12mm
8.12mm
3.88mm
340mm
14mm
14mm

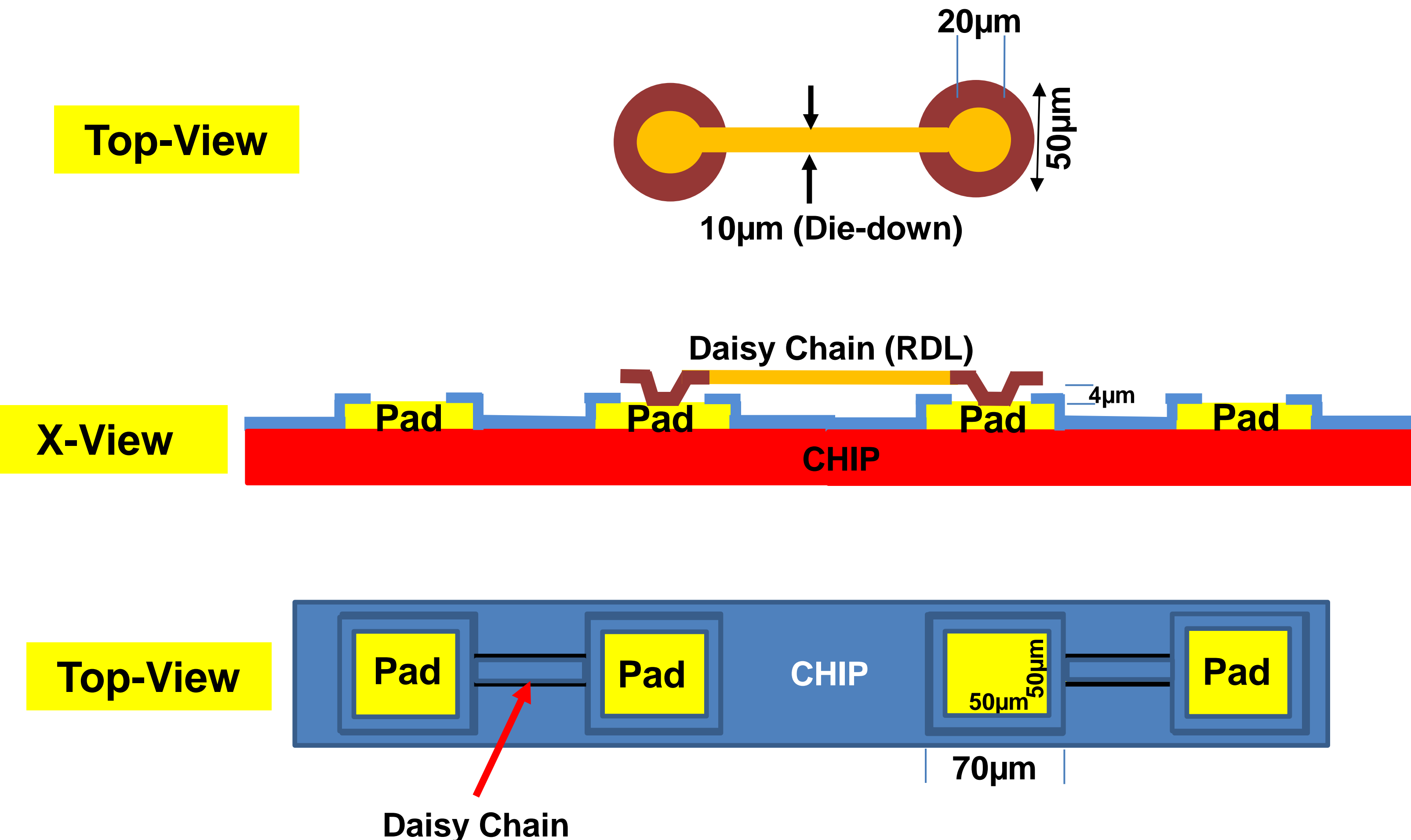
TVSiP (Phase-I)



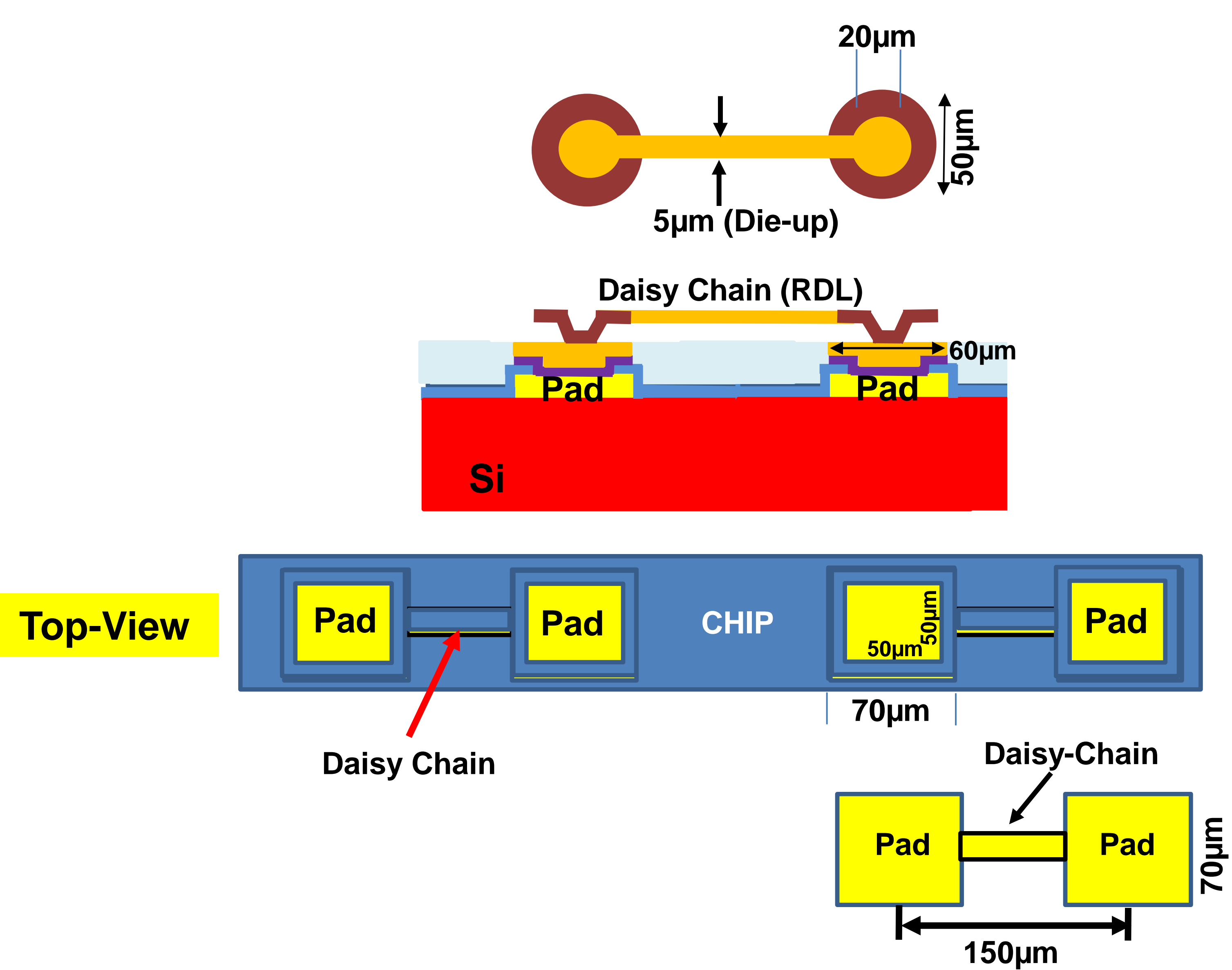
Line width/spacing of:

- 1st RDL are 10/10µm
- 2nd RDL are 15/15µm

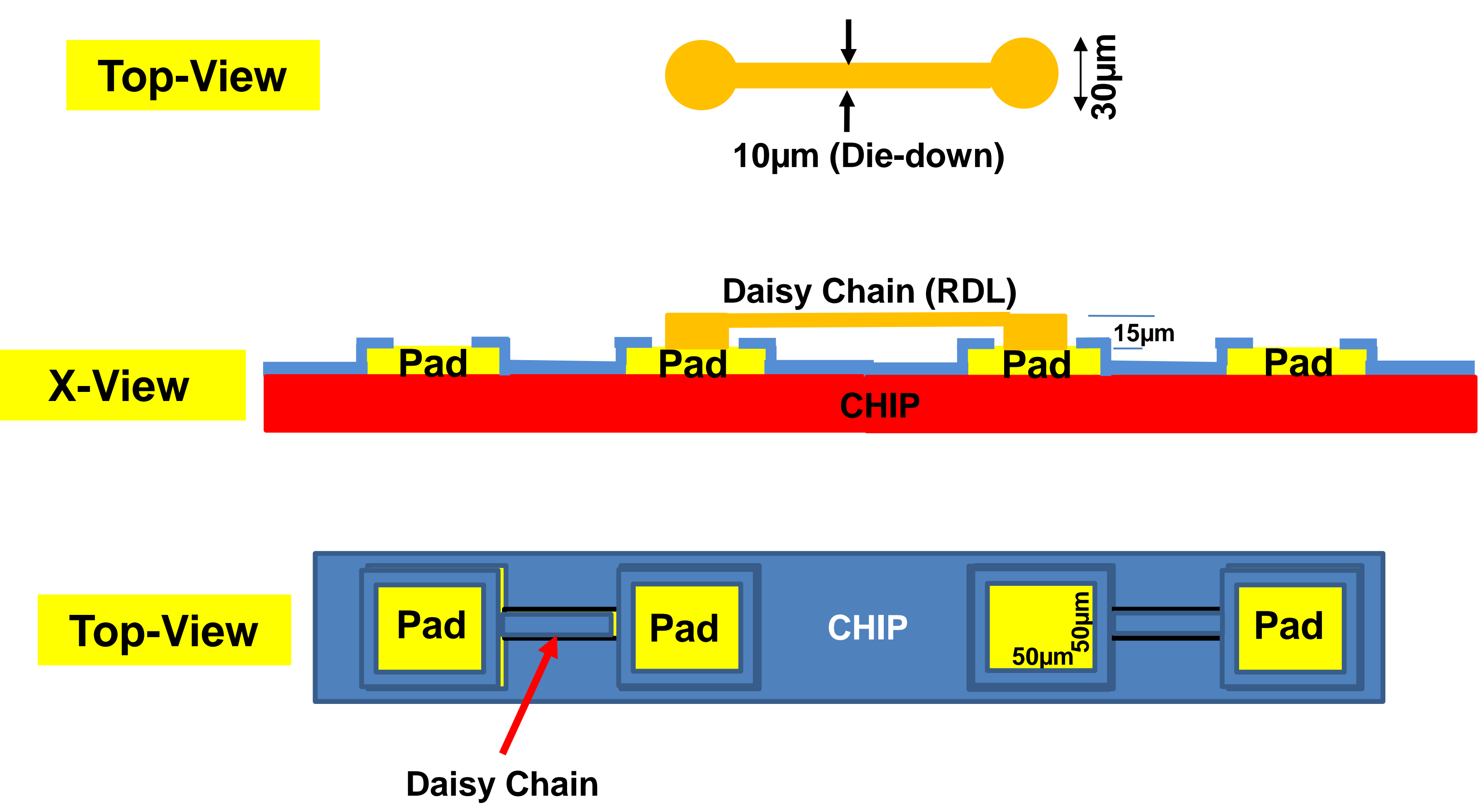
First-Layer of RDL (Die-Down) (Polymer + ECD)

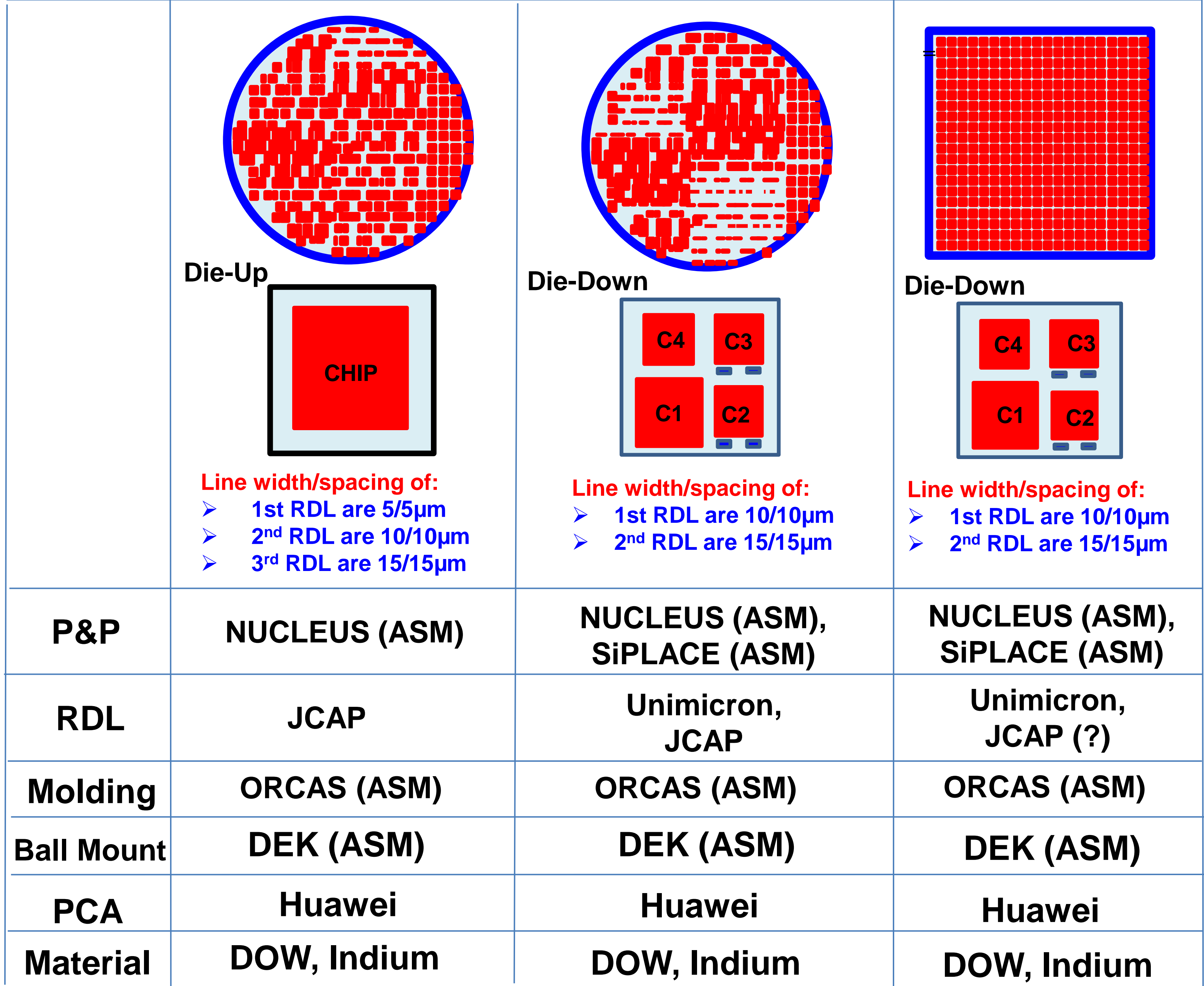


First-Layer of RDL (Die-Up)
(Polymer + ECD)



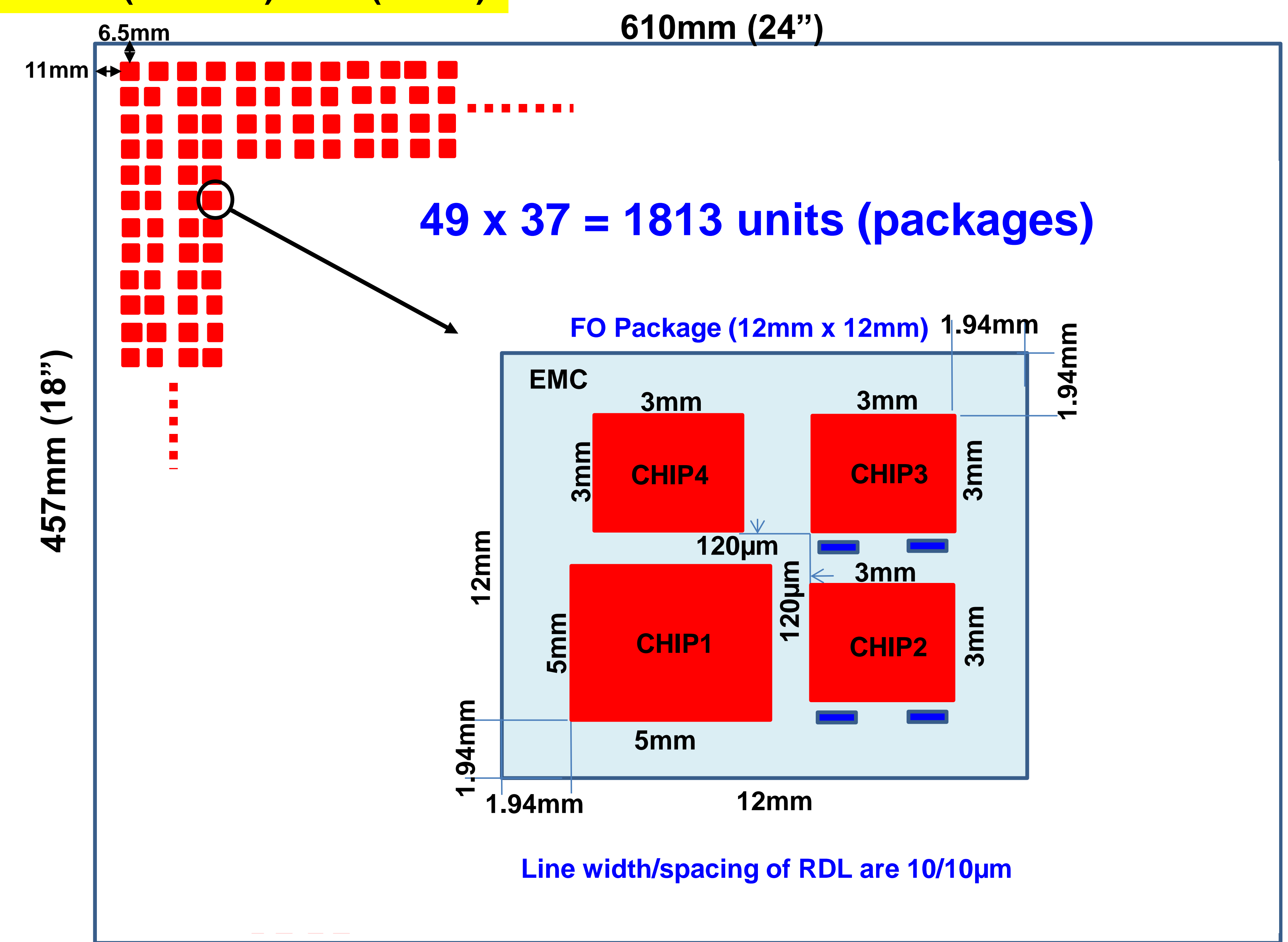
First-Layer of RDL (PCB +LDI)



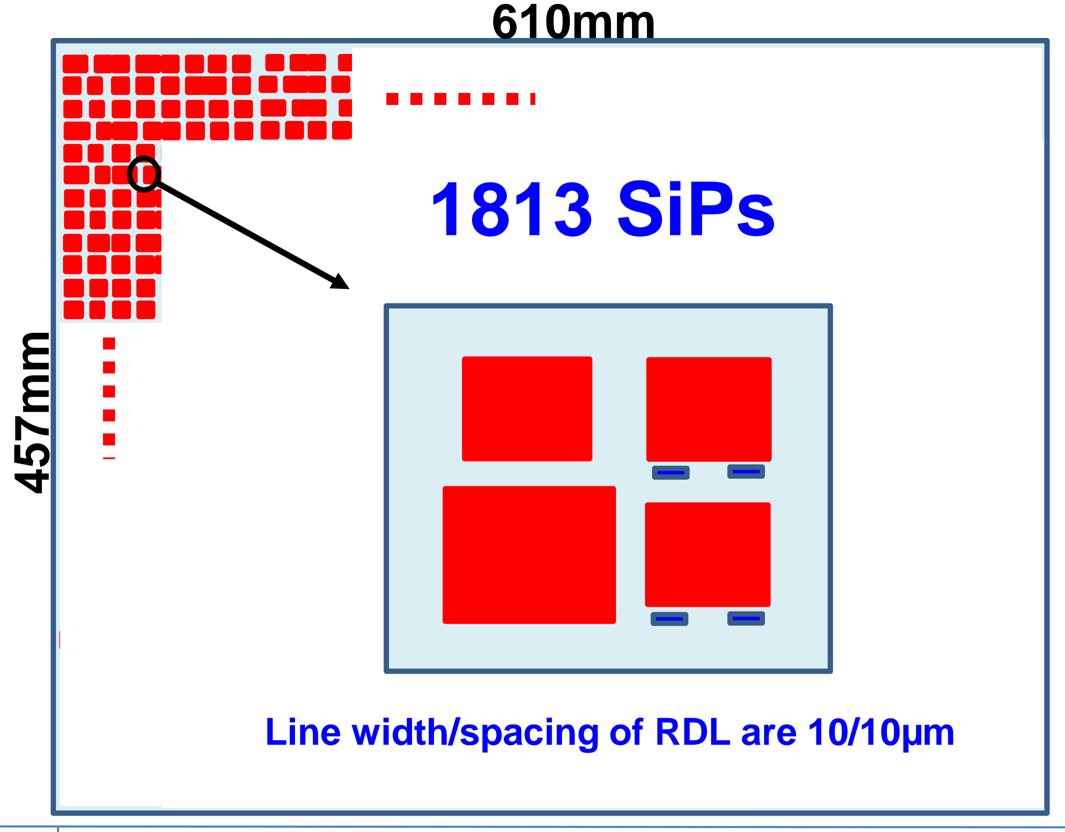


	Die-Up	Die-Down	Die-Down
	CHIP Line width/spacing of: ➢ 1st RDL are 5/5μm ➢ 2nd RDL are 10/10μm ➢ 3rd RDL are 15/15μm	C4 C3 C1 C2 Line width/spacing of: ➢ 1st RDL are 10/10μm ➢ 2nd RDL are 15/15μm	C4 C3 C1 C2 Line width/spacing of: ➢ 1st RDL are 10/10μm ➢ 2nd RDL are 15/15μm
P&P	NUCLEUS (ASM)	NUCLEUS (ASM), SiPLACE (ASM)	NUCLEUS (ASM), SiPLACE (ASM)
RDL	JCAP	Unimicron, JCAP	Unimicron, JCAP (?)
Molding	ORCAS (ASM)	ORCAS (ASM)	ORCAS (ASM)
Ball Mount	DEK (ASM)	DEK (ASM)	DEK (ASM)
PCA	Huawei	Huawei	Huawei
Material	DOW, Indium	DOW, Indium	DOW, Indium

Phase - II



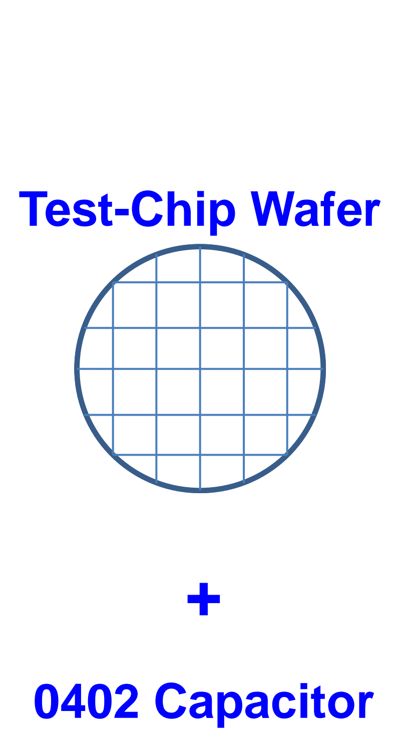
TV2PSiP (Phase-II) 1813 (49x37)
610mm (24")
6.5mm
11mm
457mm (18")
49 x 37 = 1813 units (packages)
FO Package (12mm x 12mm)
1.94mm
1.94mm
EMC
3mm
3mm
3mm
CHIP4
CHIP3
3mm
120μm
3mm
12mm
120μm
5mm
CHIP1
CHIP2
3mm
1.94mm
5mm
1.94mm
12mm
Line width/spacing of RDL are 10/10μm



P&P	NUCLEUS (ASM)	SiPLACE (ASM)
RDL	Unimicron, JCAP (?)	
Molding	ORCAS (ASM)	
Ball Mount	DEK (ASM)	
PCA	Huawei	
Material	DOW, Indium	

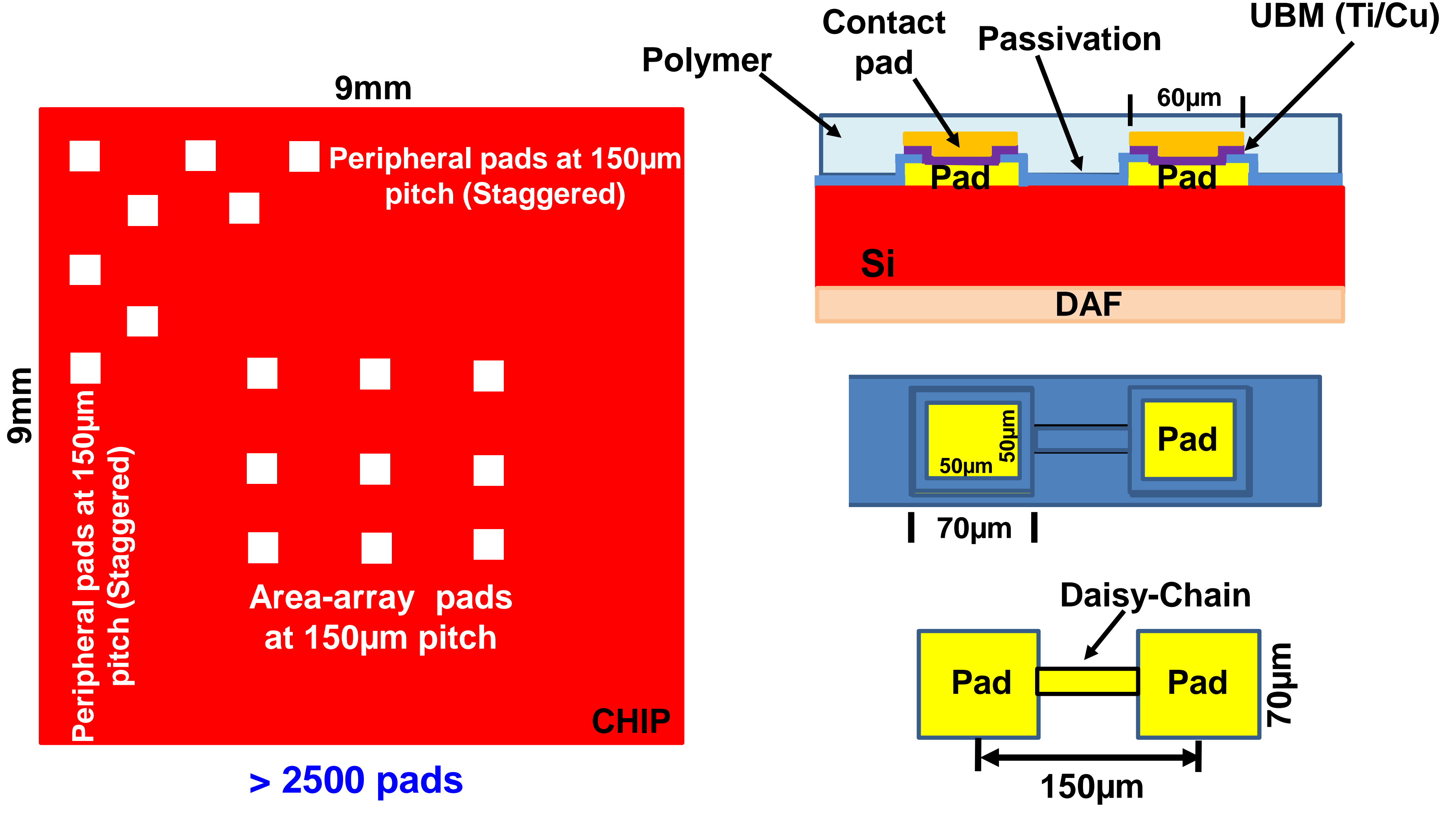
Company Task Assignments

Test-Chip Wafer Fabrication



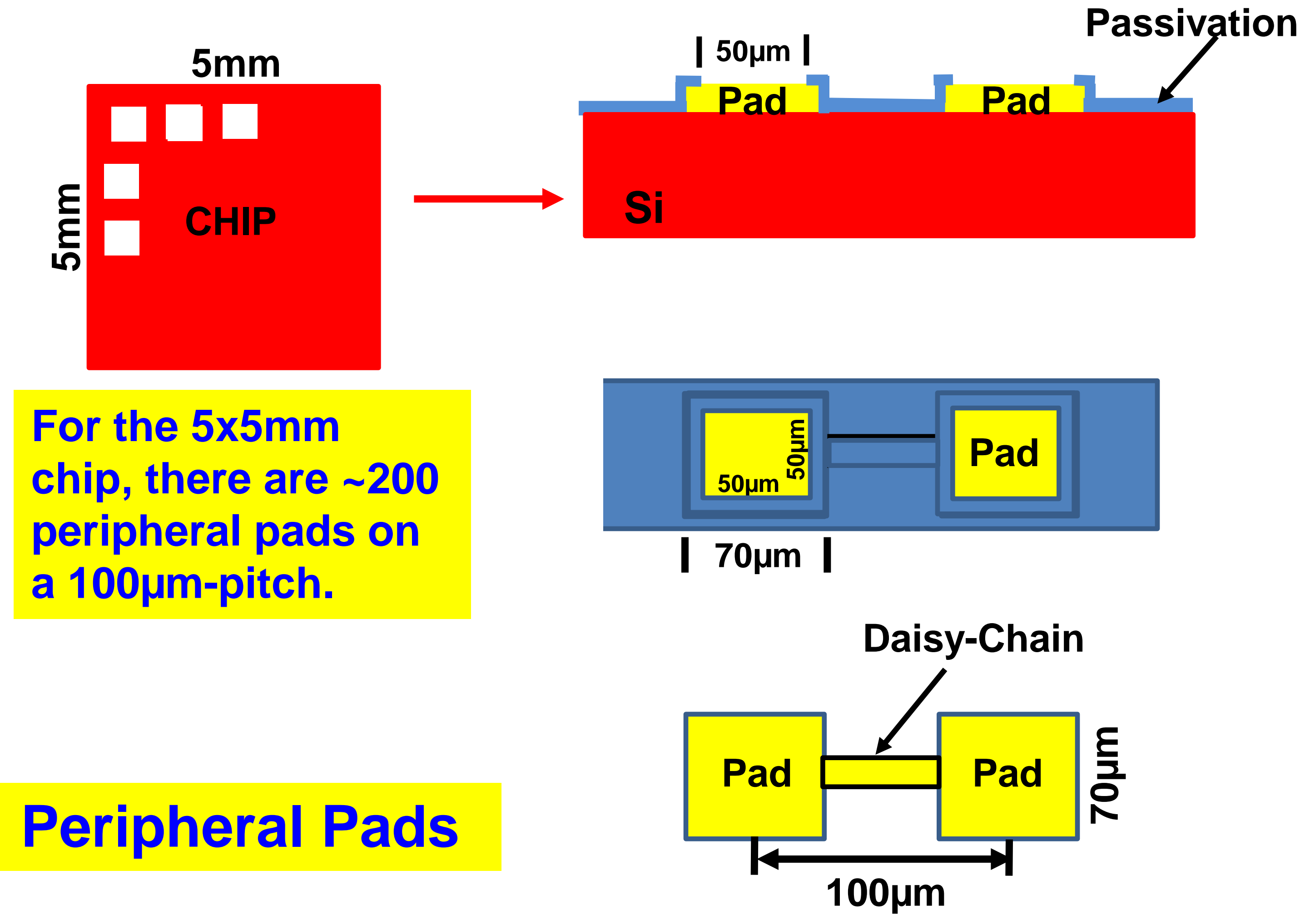
Step	Who
Layout the Test Chips	All
Fabricate the Test-Chip Wafers	❑ Sub-contract ❑ DOW provide the materials for making the test-chip wafers
Backgrind the Test-Chip Wafers	Sub-contract
Dice the Test-Chip Wafers	Sub-contract

9mm x 9mm Test Chip



Note: Before dicing the test-chip wafer, laminate a die-attach film (DAF) on the back-side of the test-chip wafer.

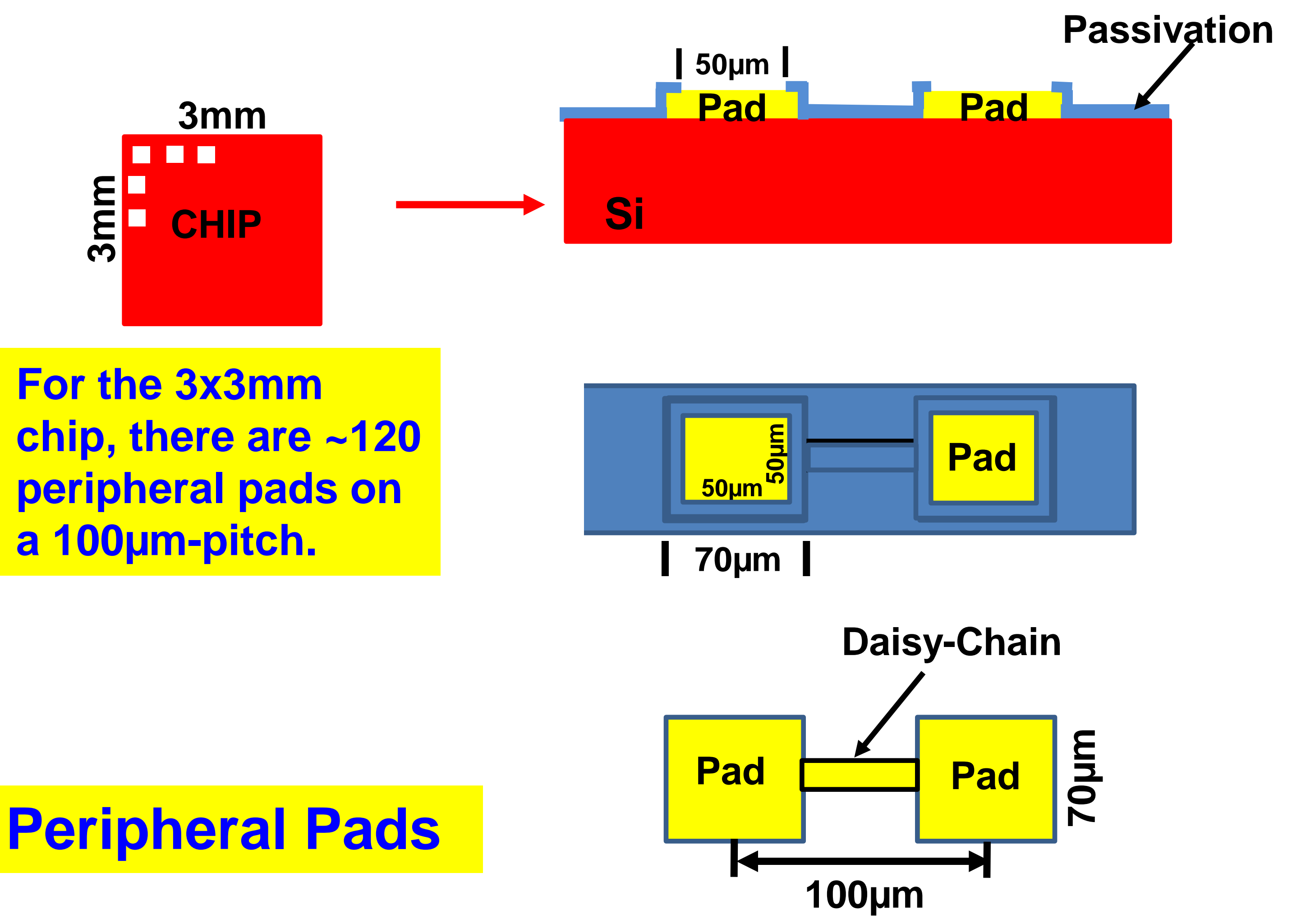
5mm x 5m Test Chip



For the 5x5mm chip, there are ~200 peripheral pads on a 100µm-pitch.

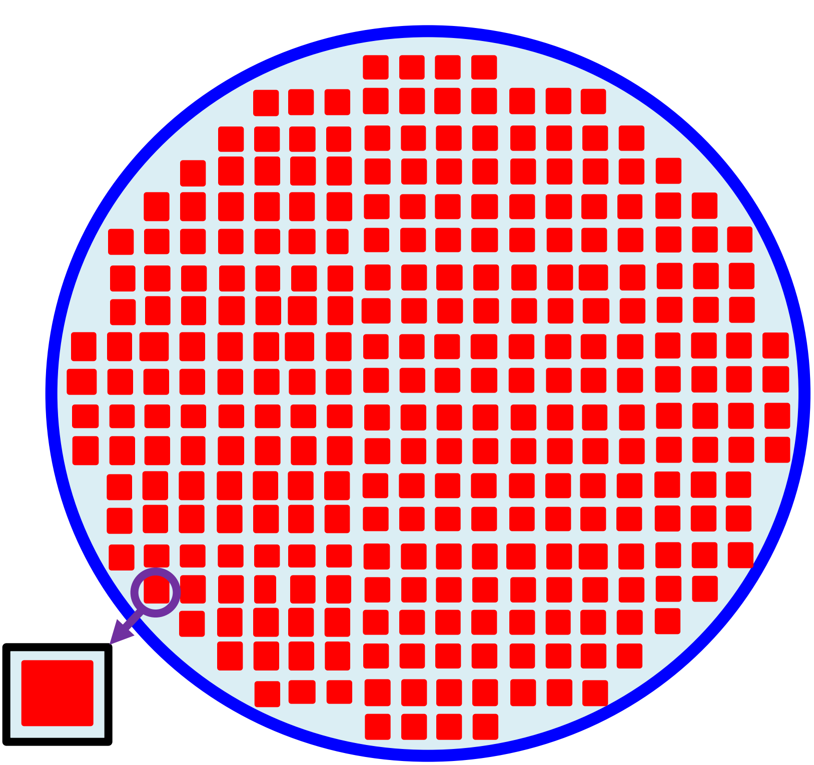
Peripheral Pads

3mm x 3mm Test Chip



Peripheral Pads

TV9W (Phase-I)
>300



- ❑ DOW provide materials on making the RDLs
- ❑ Indium provide flux on ball mounting

Glass or Si Carrier Wafer (ASM)

↓

P&P the Test Chips (face-up) on the Carrier Wafer (NUCLEUS)

↓

Compression Molding the Test Chips on Carrier Wafer (ORCAS)

↓

Backgrind the EMC and Polymer to explore the Cu Contact Pad (JCAP)

↓

Build-up the RDLs with Polymer and ECD (JCAP)

↓

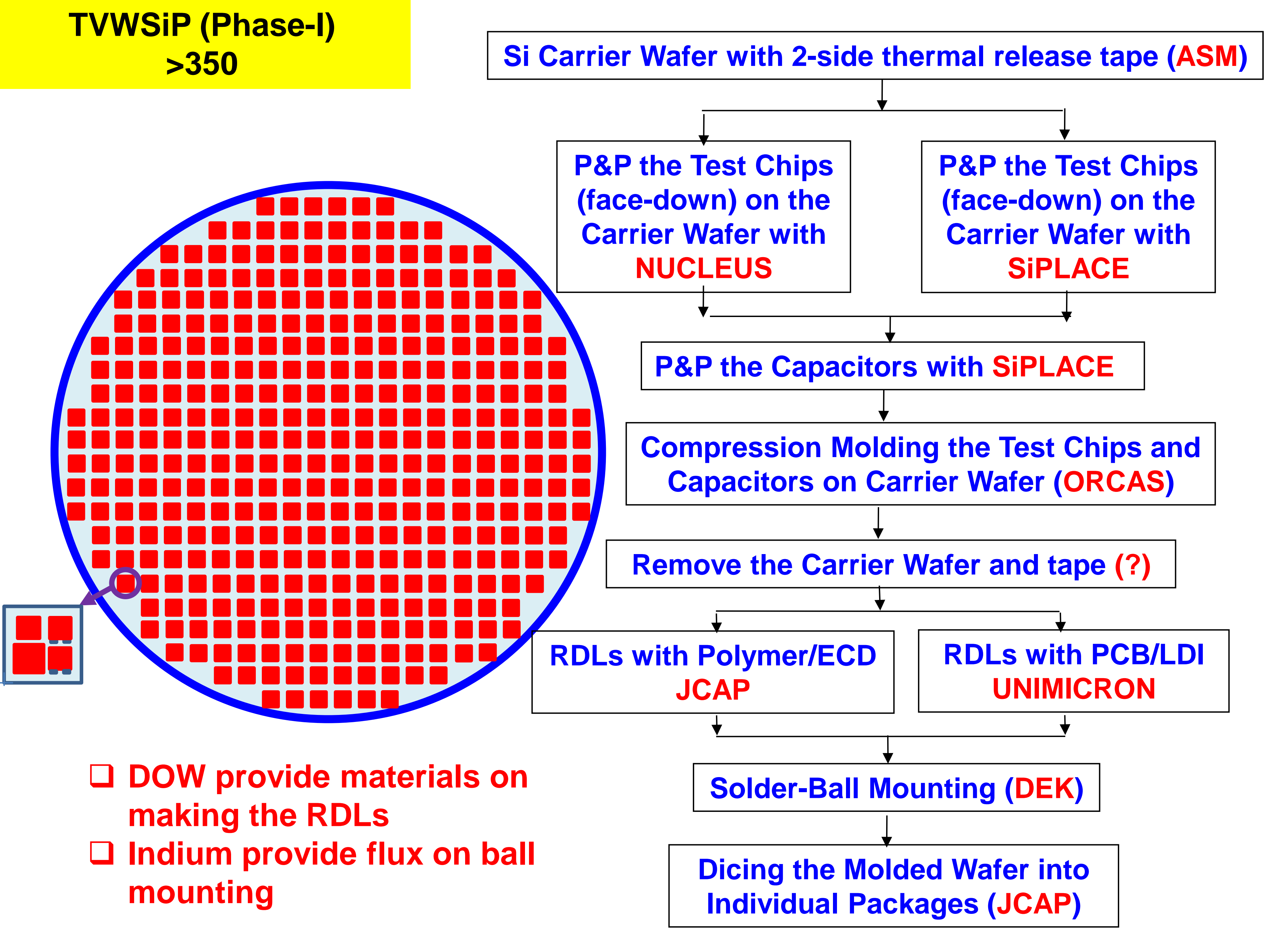
Solder-Ball Mounting (DEK)

↓

Remove the Carrier Wafer (ASM)

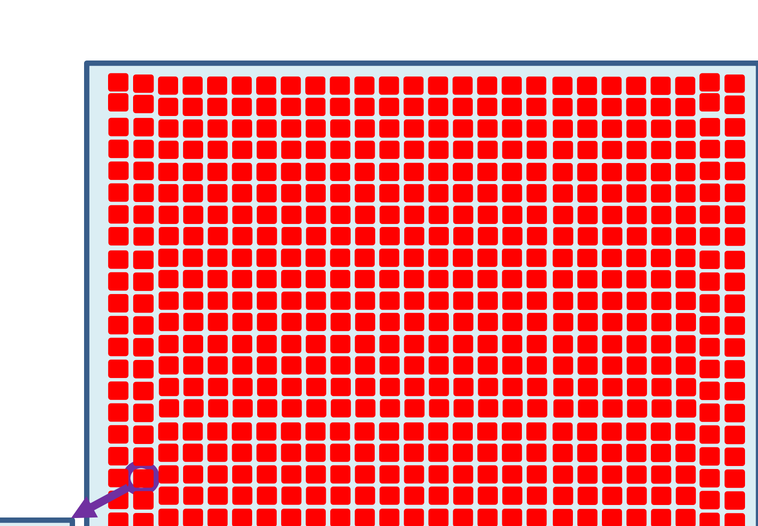
↓

Dicing the Molded Wafer into Individual Packages (JCAP)



TVWSiP (Phase-I)
>350
Si Carrier Wafer with 2-side thermal release tape (ASM)
P&P the Test Chips (face-down) on the Carrier Wafer with NUCLEUS
P&P the Test Chips (face-down) on the Carrier Wafer with SiPLACE
P&P the Capacitors with SiPLACE
Compression Molding the Test Chips and Capacitors on Carrier Wafer (ORCAS)
Remove the Carrier Wafer and tape (?)
RDLs with Polymer/ECD JCAP
RDLs with PCB/LDI UNIMICRON
Solder-Ball Mounting (DEK)
Dicing the Molded Wafer into Individual Packages (JCAP)
❑ DOW provide materials on making the RDLs
❑ Indium provide flux on ball mounting

TVPSiP (Phase-I) 676 (26x26)



Steel Panel with 2-side thermal release tape (ASM)

P&P the Test Chips (face-down) on the Panel with NUCLEUS

P&P the Test Chips (face-down) on the Panel with SiPLACE

P&P the Capacitors with SiPLACE

Compression Molding the Test Chips and Capacitors on the Panel (ORCAS)

Remove the Panel and tape (?)

RDLs with PCB/LDI UNIMICRON

RDLs with Polymer/ECD JCAP (?)

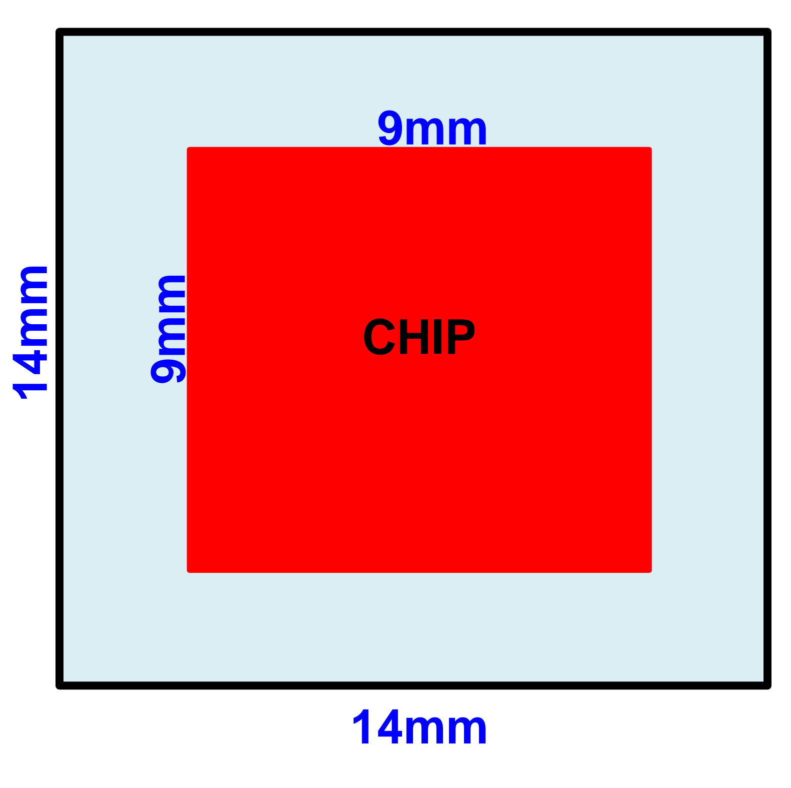
Solder-Ball Mounting (DEK)

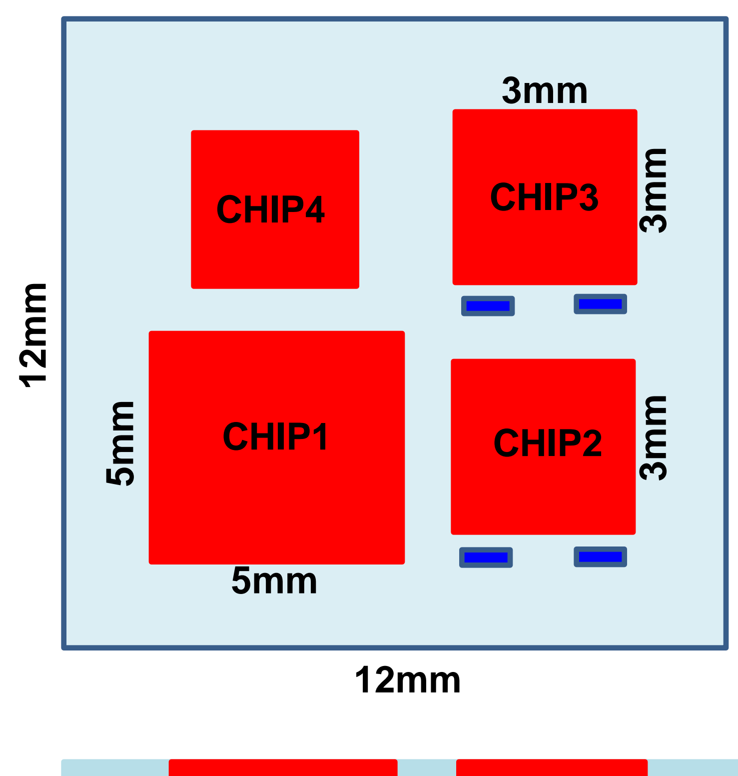
Dicing the Panel into Individual Packages (UNIMICRON)

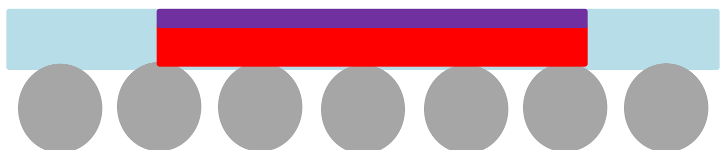
- DOW provide materials on making the RDLs
- Indium provide flux on ball mounting

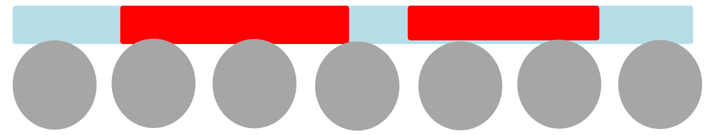
Component Qualification Test

A test socket for BGA-like packages:







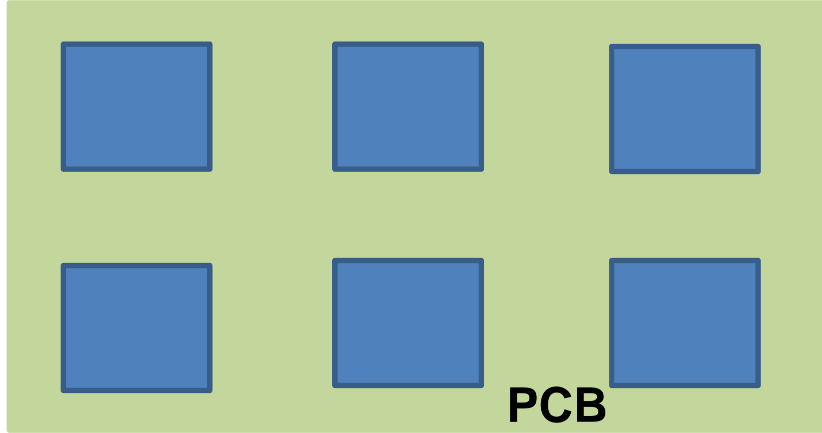


Test Board Layout, Fabrication, Assembly and Reliability Test

JESD22-B111 for Drop Test

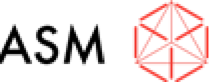
JESD22-A104D for Temperature Cycling Test

- ❑ Huawei
- ❑ Indium



Things Needed to be Discussed

- For the large chip (face-up) Die-attach film (kind, company, de-bond, shelf life, etc.)
- For the large chip (face-up) Polymer (kind, company, can the polymer backgrind with the EMC? Transparent for alignment mark?)
- Carrier materials – glass, Si, metal such as steel, etc.
- P&P accuracy for large die with fine (5µm) line width/spacing
- P&P accuracy for small die with 10µm line width/spacing
- EMC – Sumitomo (solid) and Nagase (liquid)
- RDL – JCAP say something
- RDL – Unimicron say something
- RDL – DOW say something
- Solder-Ball Mounting – DEK say something
- Removing the carrier wafer (large chip) De-bond the die-attach film
- Dicing the molded wafer into individual package
- Test socket for the 14x14mm package and the 12x12mm package
- Test board layout, fabrication, assembly, and reliability tests – Huawei and Indium
- 0402 Termination metal



Thank you very much for your attention!